Electrical Circuits LAB Term Project : Analog Computer

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Contents

CHAPTER 1 : Preliminary Work

Project Subject

- Designing an Analog Computer using OP Amps (Operational Amplifiers).

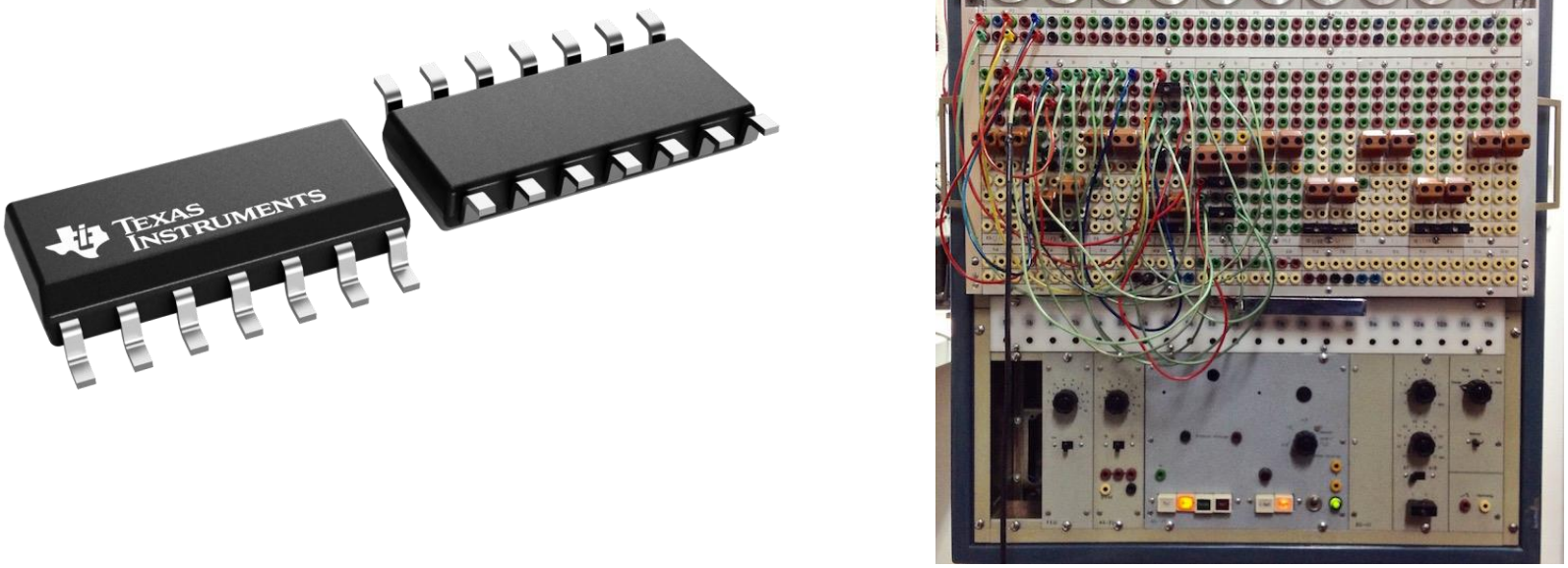


Figure 1. Texas Instruments OP-amp (Left) , GTE EA-22 Analog Computer(Right)

Source: Adapted from [1], [2]

Project Theory

- What is an OP Amp

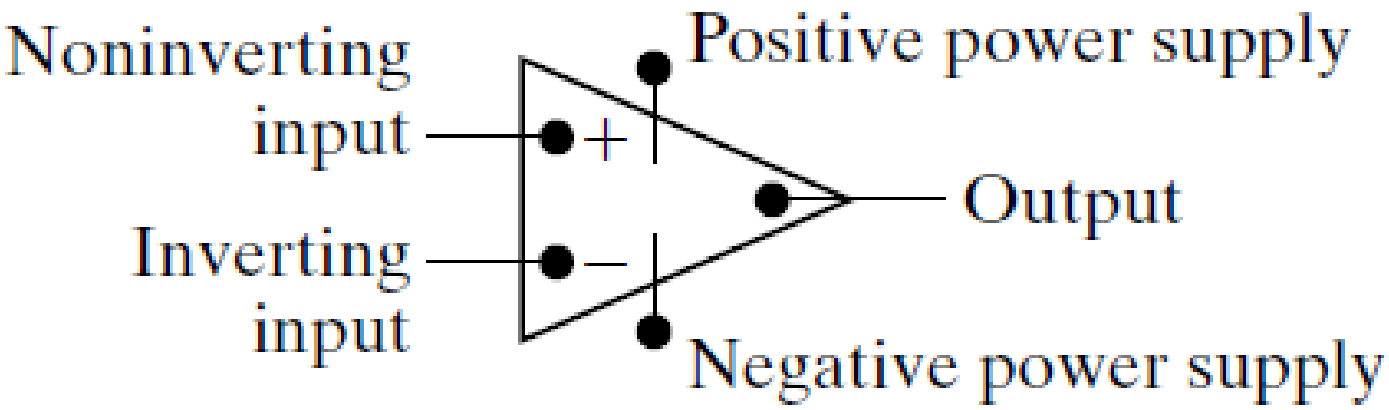
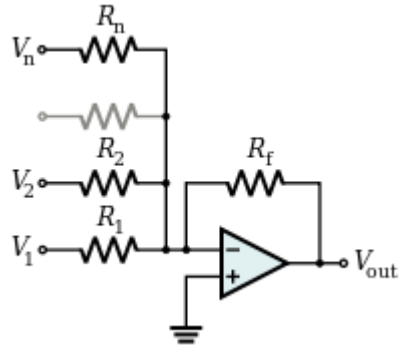


Figure 2. Circuit symbol for an operational amplifier (op amp), Source: Adapted from [4]

Project Theory (Cont.)

- Operational Amplifier Applications



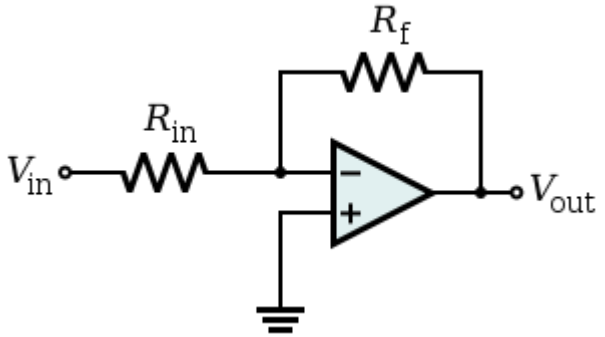
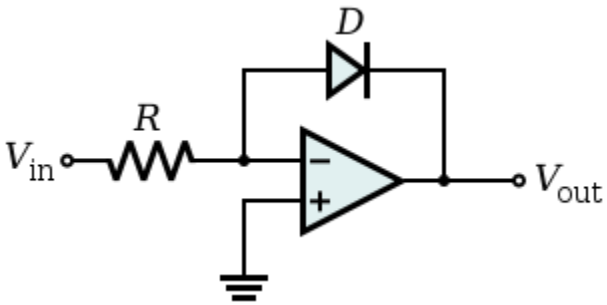


Figure 3. Summing (Left) and Inverting (Right) Operational Amplifier, Source: Adapted from [5][6]



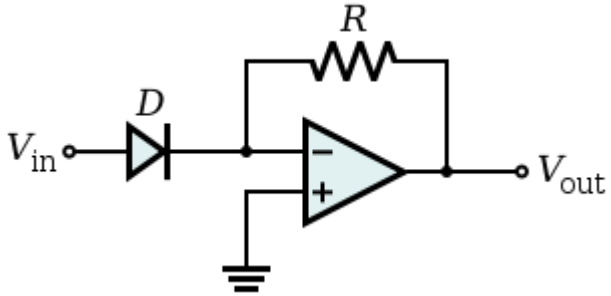


Figure 4. Log (Left) and Antilog (Right) Operational Amplifier, Source: Adapted from [5][6]

Project Theory (Cont.)

- How to implement Arithmetic Operations?

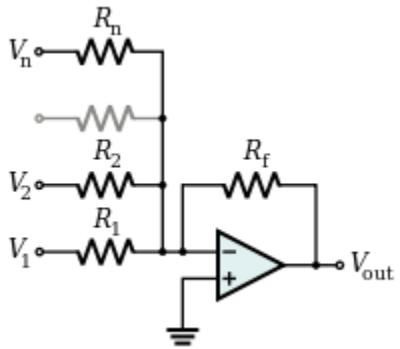


Figure 5. Summing Operational Amplifier, Source: Adapted from [6]

- Addition
  - Just input two Voltages Using the Summing Operational Amplifier

Project Theory (Cont.)

- How to implement Arithmetic Operations?

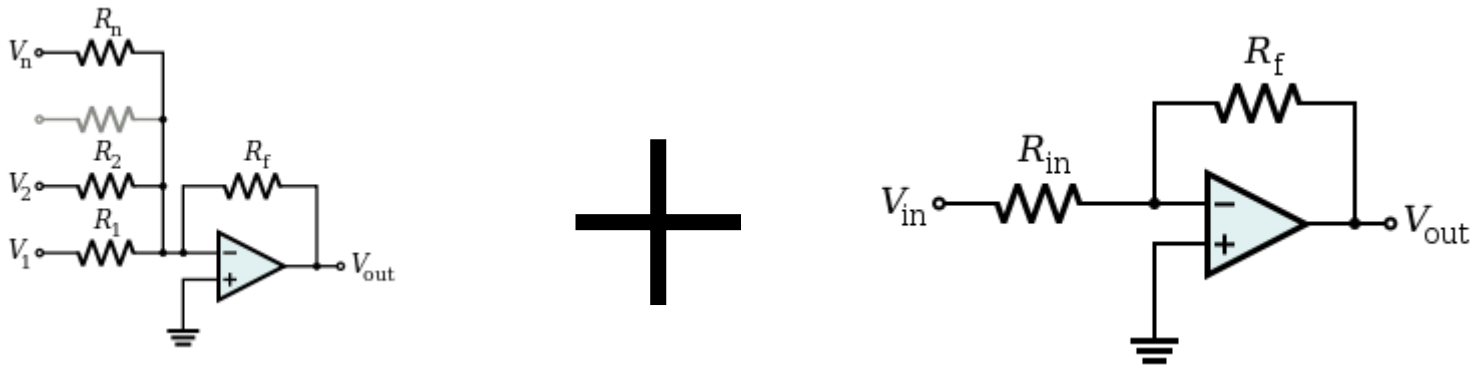


Figure 6. Summing (Left) and Inverting Operational Amplifier, Source: Adapted from [6]

- Subtraction
  - Step 1. Invert one input using the Inverting Operational Amplifier
  - Step 2. Sum the two inputs using the Summing Operational Amplifier

Project Theory (Cont.)

- How to implement Arithmetic Operations?

- As we know addition in logarithmic operations is multiplication and subtraction in logarithmic operations is division.

$$\log a - \log b = \log\left(\frac{a}{b}\right) \quad \log a + \log b = \log(ab)$$

- We also know that logarithmic values are the inverse of the exponential values.

$$\log_a b = y \Leftrightarrow a^y = b$$

- We will use these properties to implement multiplication and division.

Project Theory (Cont.)

- How to implement Arithmetic Operations?

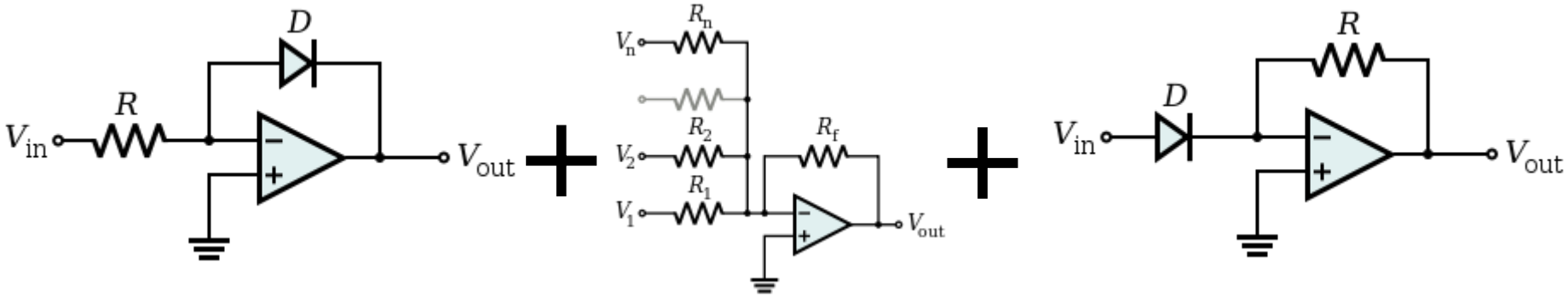


Figure 7. Log (Left), Summing (Middle) and Antilog (Right) Operational Amplifier, Source: Adapted from [5][6]

- Multiplication
  - Step 1. Scale both the inputs to logarithmic values
  - Step 2. Sum the two inputs using the Summing Operational Amplifier
  - Step 3. Scale them back to before the logarithmic values using exponential scale

Project Theory (Cont.)

- How to implement Arithmetic Operations?

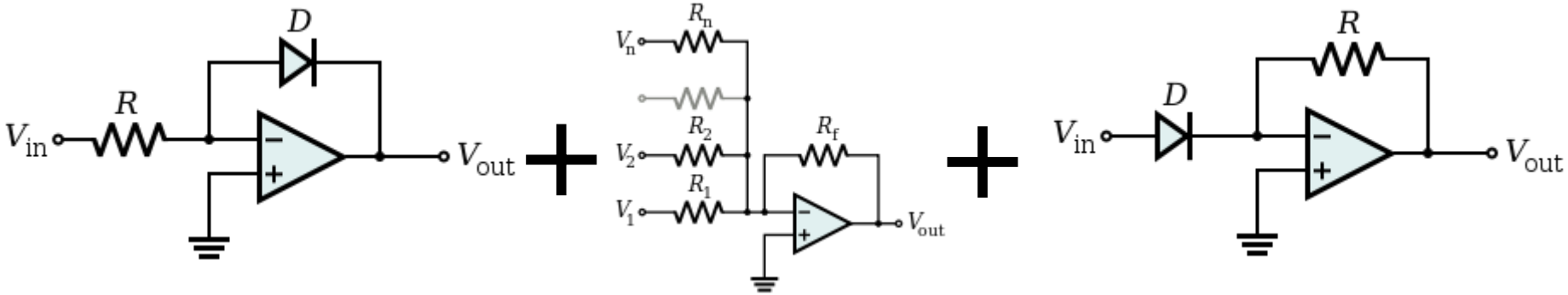


Figure 8. Log (Left), Summing (Middle) and Antilog (Right) Operational Amplifier, Source: Adapted from [5][6]

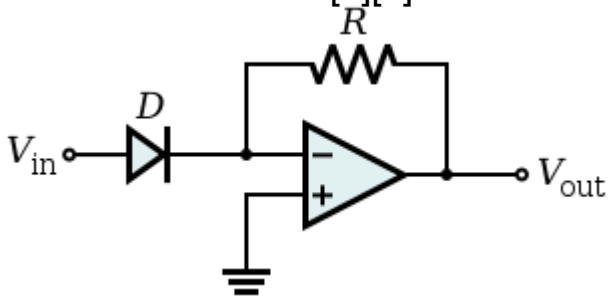
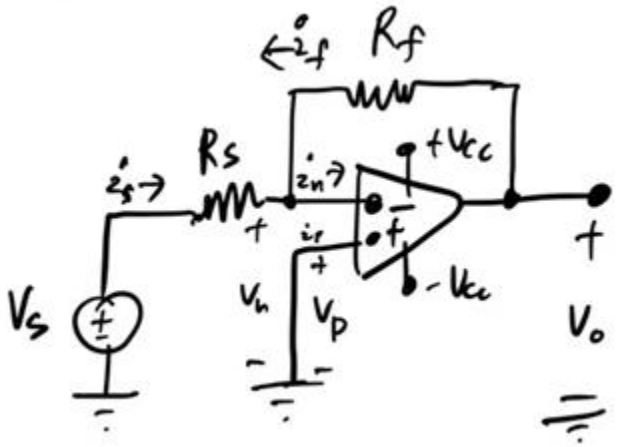


Figure 9. Antilog Operational Amplifier, Source: Adapted from [5]

- Division
  - Step 1. Scale both the inputs to logarithmic values
  - Step 2. Invert one input using the Inverting Operational Amplifier
  - Step 3. Sum the two inputs using the Summing Operational Amplifier
  - Step 3. Scale them back to before the logarithmic values using exponential scale

Project Theory (Cont.)

- Theoretical Calculations for each Circuit



$$\dot{i}_s + \dot{i}_f - \dot{i}_n = 0 \quad \cdots\cdots ①$$

where $V_p = 0$, therefore $V_n = V_p = 0$

$$\dot{i}_s = \frac{V_s}{R_s}, \quad \dot{i}_f = \frac{V_o}{R_f} \quad \cdots ②, ③$$

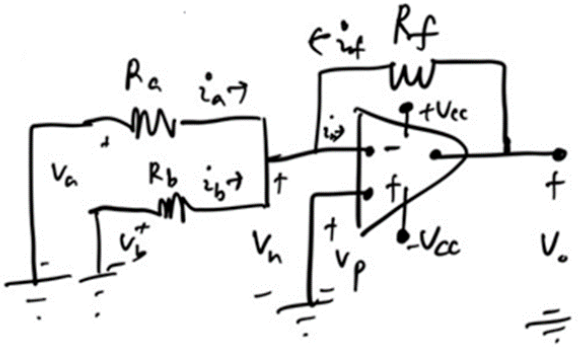
$V_n = V_p = 0$ for constraints.

substitute ②, ③ in ①

$$\frac{V_s}{R_s} + \frac{V_o}{R_f} - 0 = 0$$

$$V_o = -\frac{R_f}{R_s} V_s$$

Figure 10. Inverting Operational Amplifier, Source: Made from Notability



$$\dot{i}_a + \dot{i}_b + \dot{i}_n + \dot{i}_f = 0$$

$$\frac{V_n - V_a}{R_a} + \frac{V_n - V_b}{R_b} + \frac{V_n - V_o}{R_f} = 0$$

$$V_o = -\left(\frac{R_f}{R_a} V_a + \frac{R_f}{R_b} V_b\right)$$

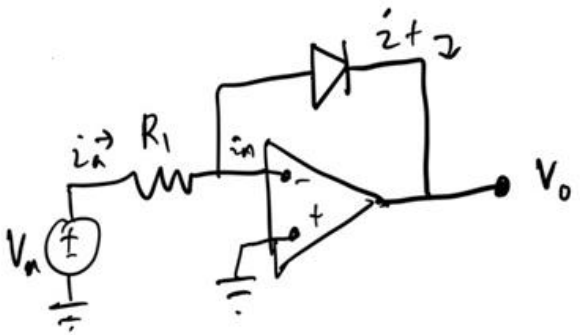
if $R_a = R_b = R_s$ then

$$V_o = -\frac{R_f}{R_s}(V_a + V_b)$$

Figure 11. Summing Operational Amplifier, Source: Made from Notability

Project Theory (Cont.)

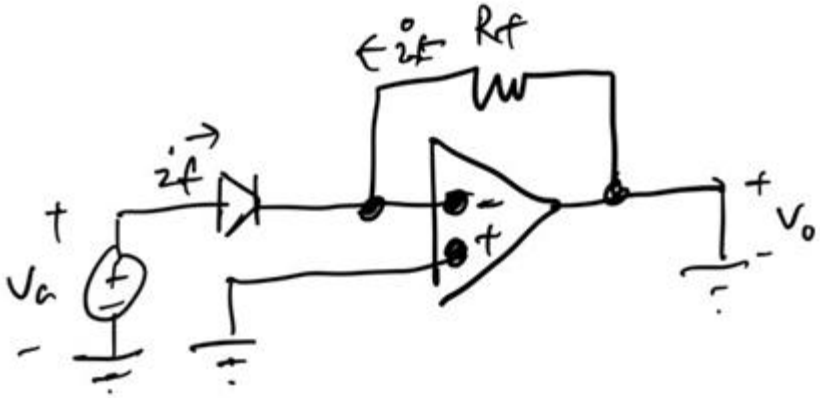
- Theoretical Calculations for each Circuit



$$i_a - i_f - i_n = 0 \quad \cdots (1)$$
$$i_a = \frac{V_a}{R_1} \quad \cdots (2)$$
$$i_f = i_s e^{\left(\frac{V_o}{V_T}\right)} \quad \cdots (3)$$

$$i_a = i_f$$
$$i_a = i_s e^{\left(\frac{V_o}{V_T}\right)}$$
$$\frac{i_a}{i_s} = e^{\frac{V_o}{V_T}}$$
$$\ln\left(\frac{i_a}{i_s}\right) = \frac{V_o}{V_T}$$
$$V_o = V_T \ln\left(\frac{i_a}{i_s}\right) \text{ since } V_{out} = -V_o$$
$$V_{out} = -V_T \ln\left(\frac{i_a}{i_s}\right) \text{ and } i_a = \frac{V_a}{R_1}$$
$$V_{out} = -V_T \ln\left(\frac{V_a}{i_s R_1}\right)$$

Figure 12. Log Operational Amplifier, Source: Made from Notability



$$i_f + i_F + i_n = 0$$
$$i_F = \frac{V_o - 0}{R_f}$$
$$i_f + \frac{V_o}{R_f} = 0$$
$$i_f = -\frac{V_o}{R_f}$$
$$V_o = -R_f i_f \text{ where } i_f = i_s e^{\left(\frac{V_a}{V_T}\right)}$$
$$= -R_f i_s e^{\left(\frac{V_a}{V_T}\right)}, \; V_o = V_a \rightarrow V_o = -R_f i_s e^{\left(\frac{V_a}{V_T}\right)}$$

Figure 13. Antilog Operational Amplifier, Source: Made from Notability

Project Theory (Cont.)

- Theoretical Calculations for each Circuit

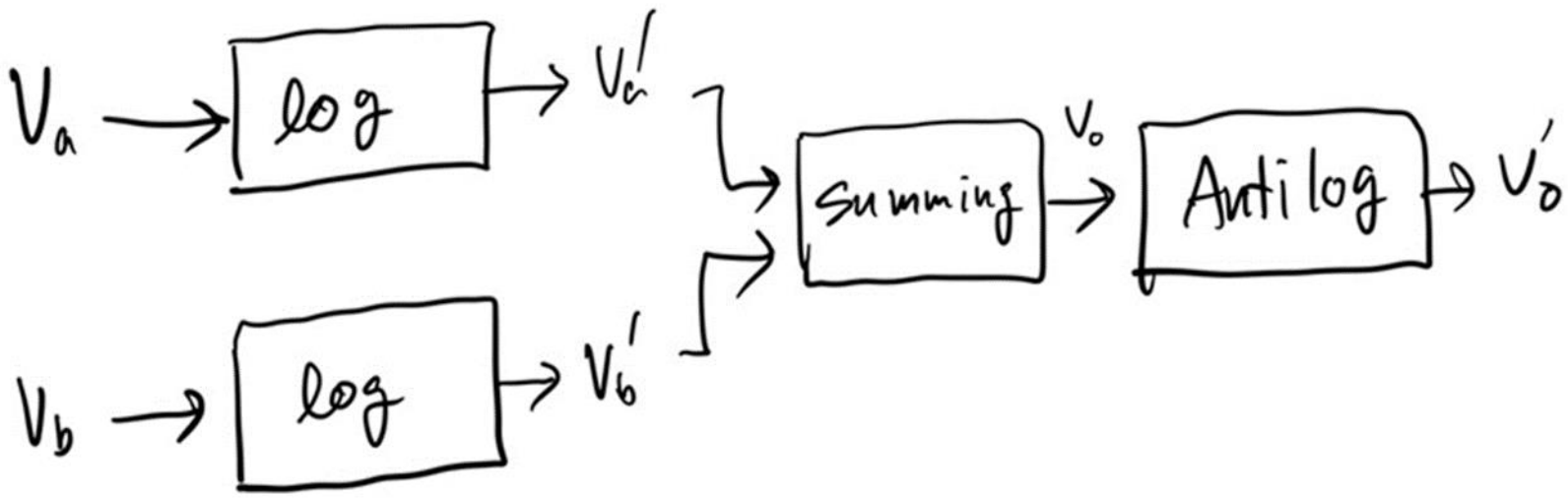


Figure 14. Multiplication, Source: Made from Notability

$$\log: V_o = -V_T \ln\left(\frac{V_i}{I_S R}\right), \quad \text{Antilog}: V_o = -I_S R e^{\left(\frac{V_i}{V_T}\right)}$$

Project Theory (Cont.)

- Theoretical Calculations for each Circuit

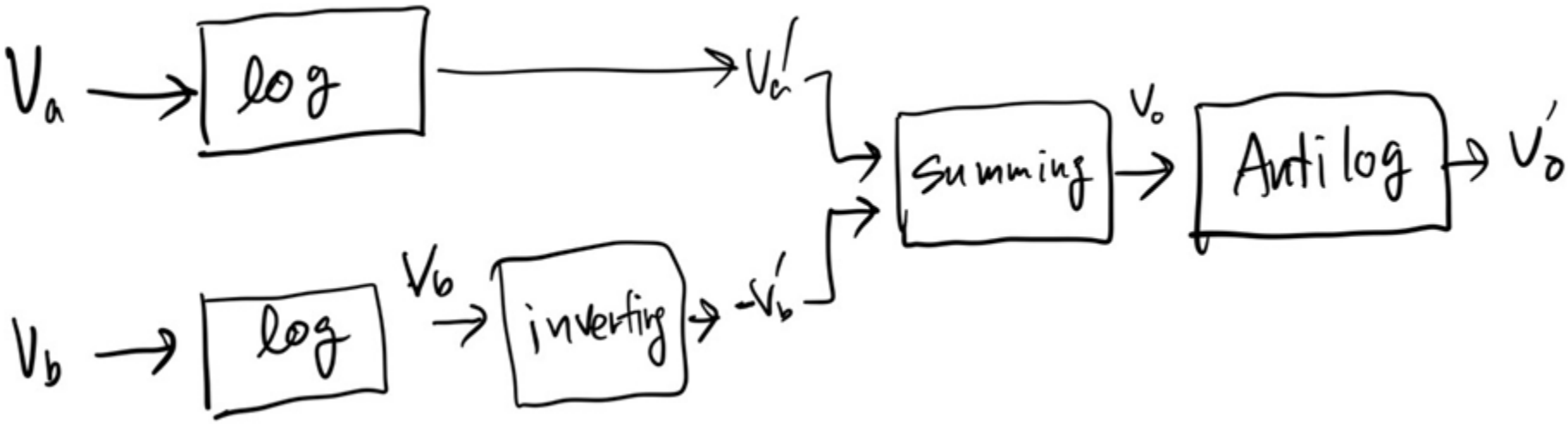


Figure 15. Division, Source: Made from Notability

$$\log : V_o = -V_T \ln\left(\frac{V_i}{I_S R}\right), \quad \text{Antilog} : V_o = -I_S R e^{\left(\frac{V_i}{V_T}\right)}$$

Project Theory (Cont.)

- Theoretical Calculations for each Circuit

log : $V_o = -V_T \ln\left(\frac{V_i}{I_S R}\right)$, Antilog : $V_o = -I_S R e^{\left(\frac{V_i}{V_T}\right)}$

$v_a' = -V_T \ln\left(\frac{V_a}{I_S R}\right)$, $V_b' = -V_T \ln\left(\frac{V_b}{I_S R}\right)$

$V_C = -(V_a + V_b) = V_T \ln\left(\frac{V_a}{I_S R}\right) + V_T \ln\left(\frac{V_b}{I_S R}\right)$

$= V_T \ln\left(\frac{V_a V_b}{(I_S R)^2}\right)$

$V_o = -I_S R e^{(V_i/V_T)} = -I_S R e^{\frac{V_T}{V_T} \ln\left(\frac{V_a V_b}{(I_S R)^2}\right)}$

$= -I_S R \frac{V_a V_b}{(I_S R)^2} = -\frac{V_a V_b}{I_S R}$

$v_a' = -V_T \ln\left(\frac{V_a}{I_S R}\right)$, $V_b' = V_T \ln\left(\frac{V_b}{I_S R}\right)$

$V_C = -(V_a + V_b) = V_T \ln\left(\frac{V_a}{I_S R}\right) - V_T \ln\left(\frac{V_b}{I_S R}\right)$

$= V_T \ln\left(\frac{V_a}{V_b}\right)$

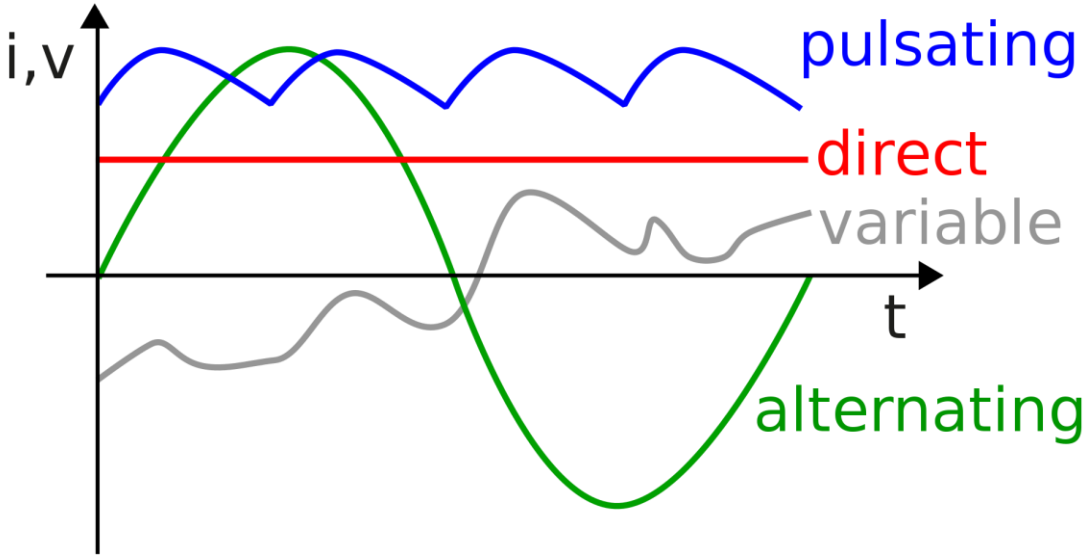
$V_o = -I_S R e^{(V_i/V_T)} = -I_S R e^{\frac{V_T}{V_T} \ln\left(\frac{V_a}{V_b}\right)}$

$= -I_S R \frac{V_a}{V_b}$

Figure 16. Multiplication (Left) Division (Right), Source: Made from Notability

Project Theory (Cont.)

- How to make a Power Supply with Constant Voltage?



- Spec of Power Supply :
- 1. Need DC Voltage
- 2. Need Both : +12 Volts and -12 Volts

Figure 17. Various Signals, Source: Adapted from [10]

Project Theory (Cont.)

- How to make a Power Supply with Constant Voltage?

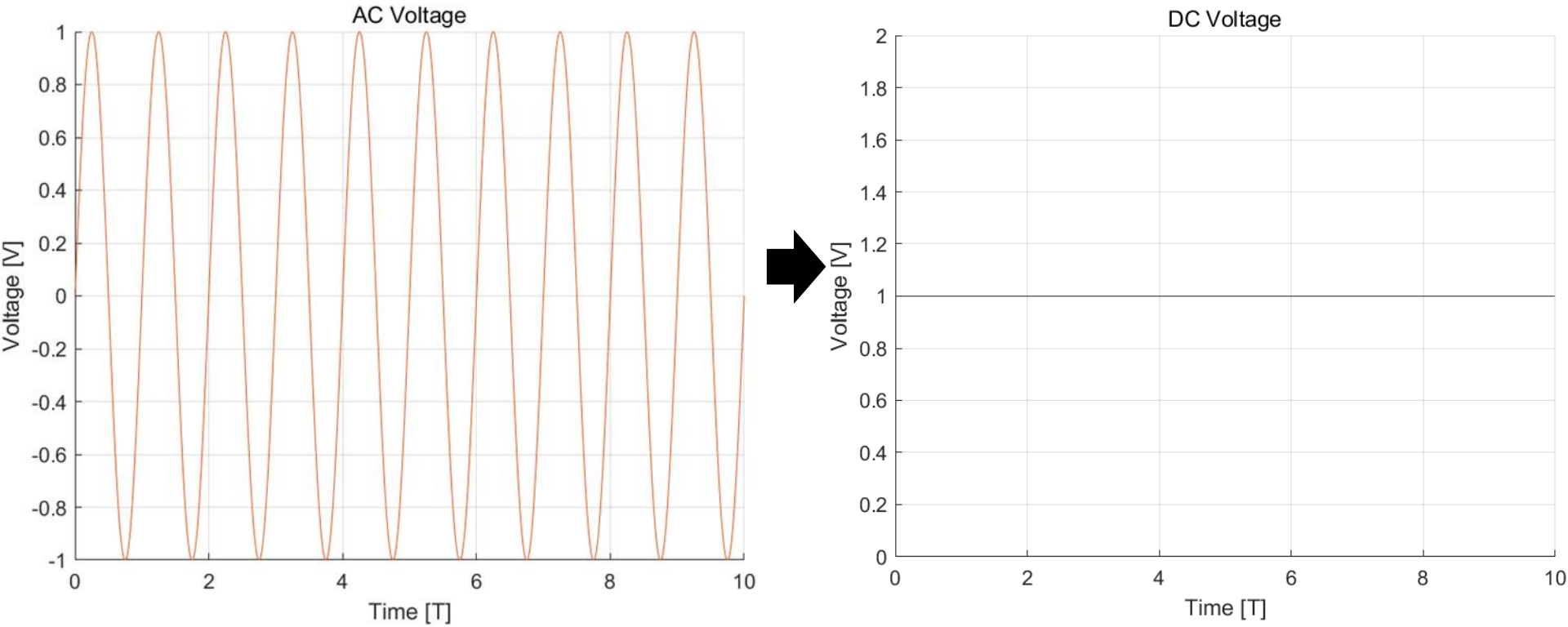


Figure 18. AC Voltage (Left) and DC Voltage (Right), Source: Adapted from [11]

- We need DC voltage for input!

Project Theory (Cont.)

- How to make a Power Supply with Constant Voltage?

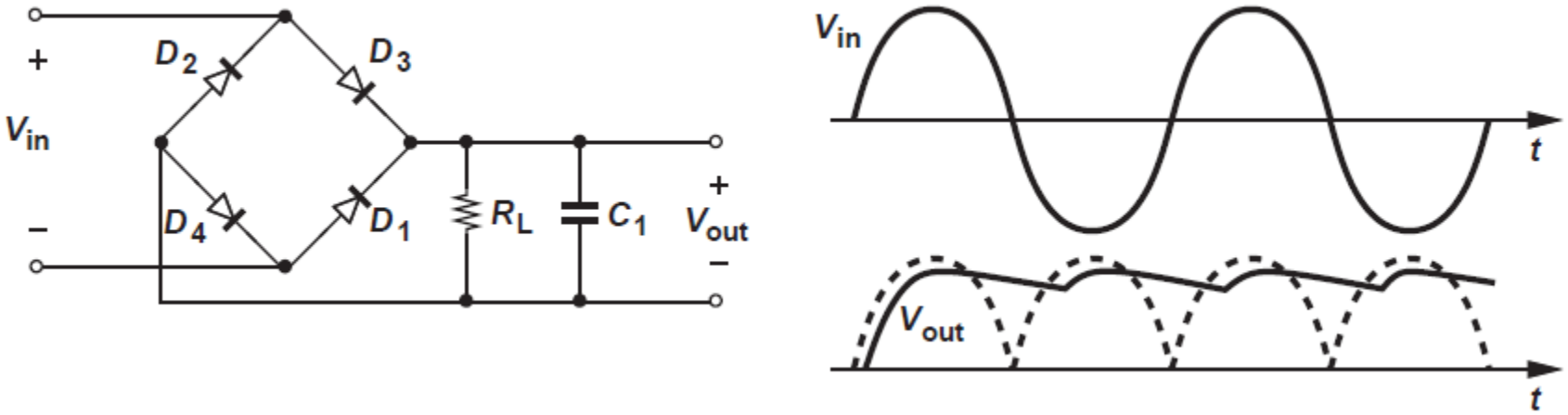


Figure 19. Full – Wave Rectifier Circuit, Source: Adapted from [9]

$$V_R \approx \frac{1}{2} \cdot \frac{V_p - 2V_{D,on}}{R_L C_1 f_{in}}$$

- Ripple Voltage

- For Constant Voltage we need to reduce the Ripple Voltage!

Project Theory (Cont.)

- How to make a Power Supply with Constant Voltage?

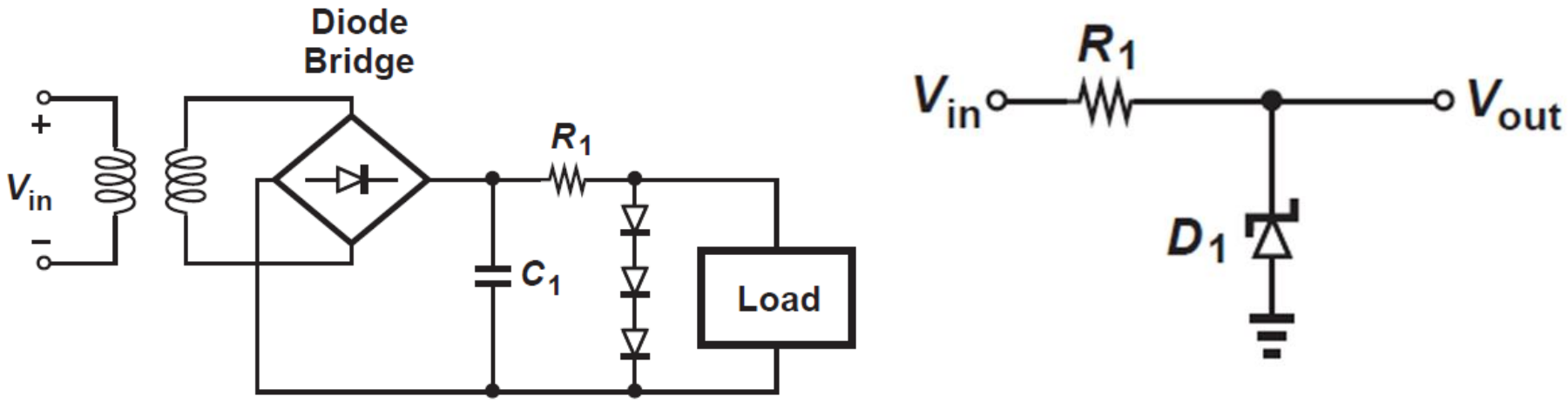


Figure 20. Voltage Regulation using a Zener Diode, Source: Adapted from [9]

Project Theory (Cont.)

- How to make a Power Supply with Constant Voltage?

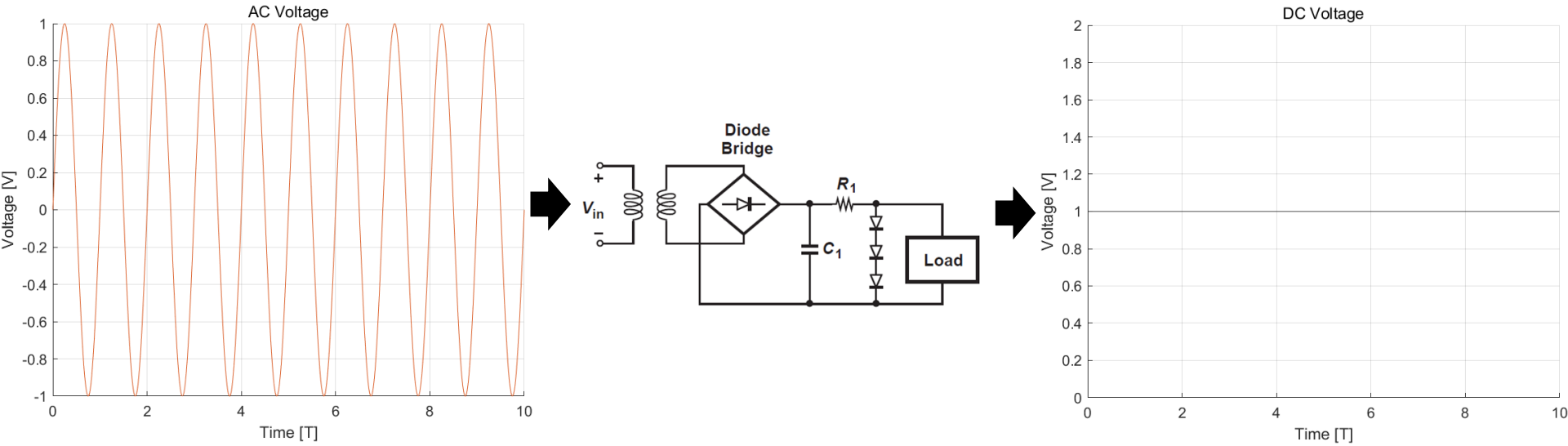


Figure 21. Overall Power Supply Design, Source: Adapted from [9][11]

Project Theory (Cont.)

- Used Parts for the Project

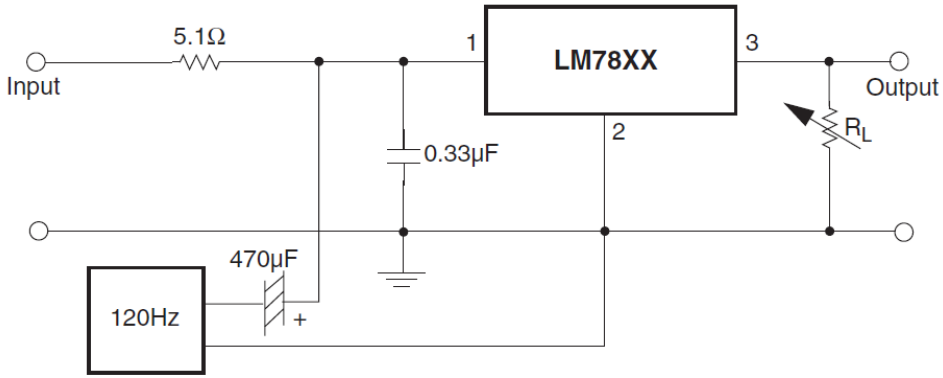


Figure 9. Ripple Rejection

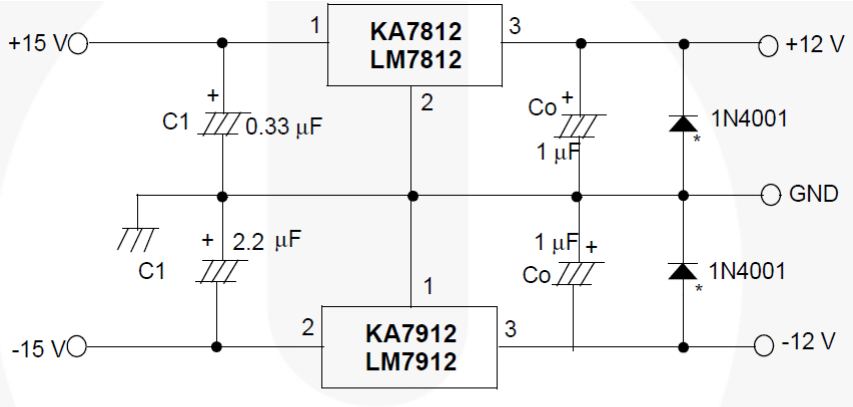


Figure 8. Split Power Supply (±12 V / 1 A)

Figure 22. LM7812 Datasheet (Left) LM7912 Datasheet (Right) , Source: Adapted from [7][8]

Project Simulation

- Computer Simulation for each Circuit

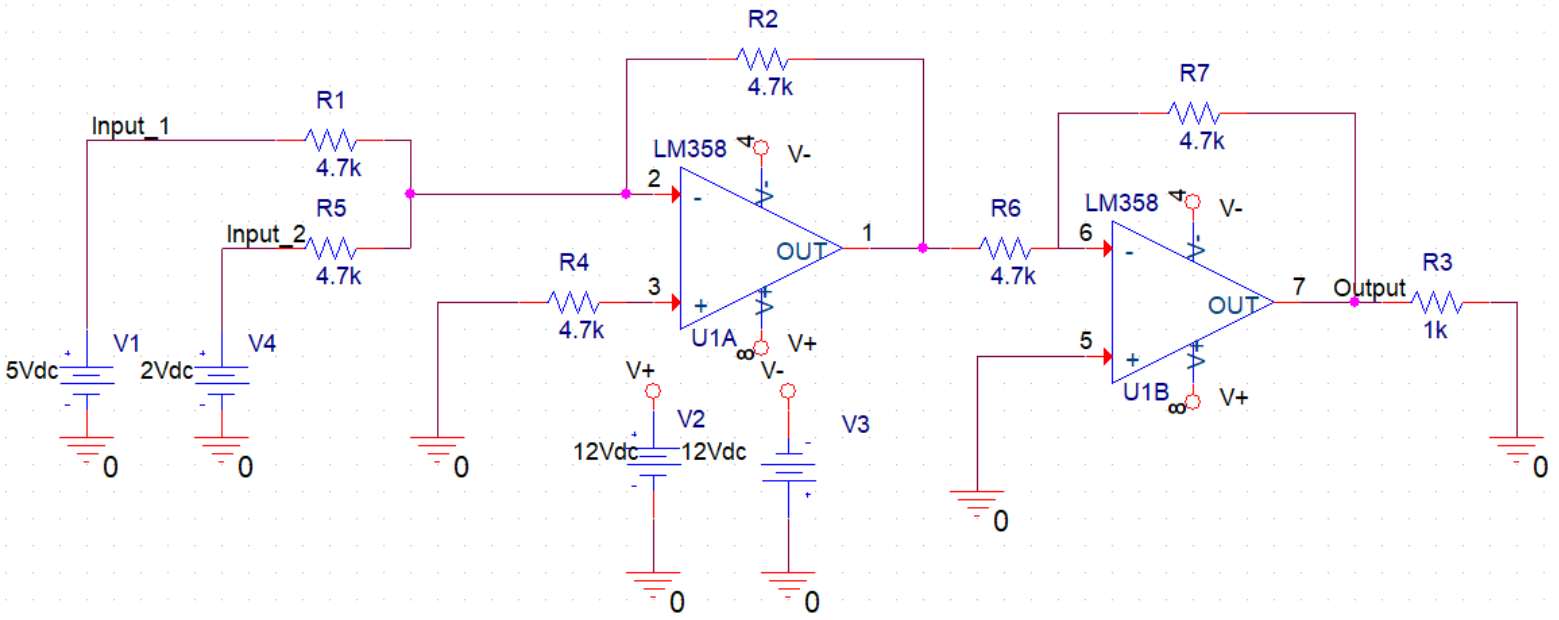


Figure 23. Pspice Addition Circuit Schematic, Source: Adapted from [3]

Project Simulation (Cont.)

- Computer Simulation for each Circuit

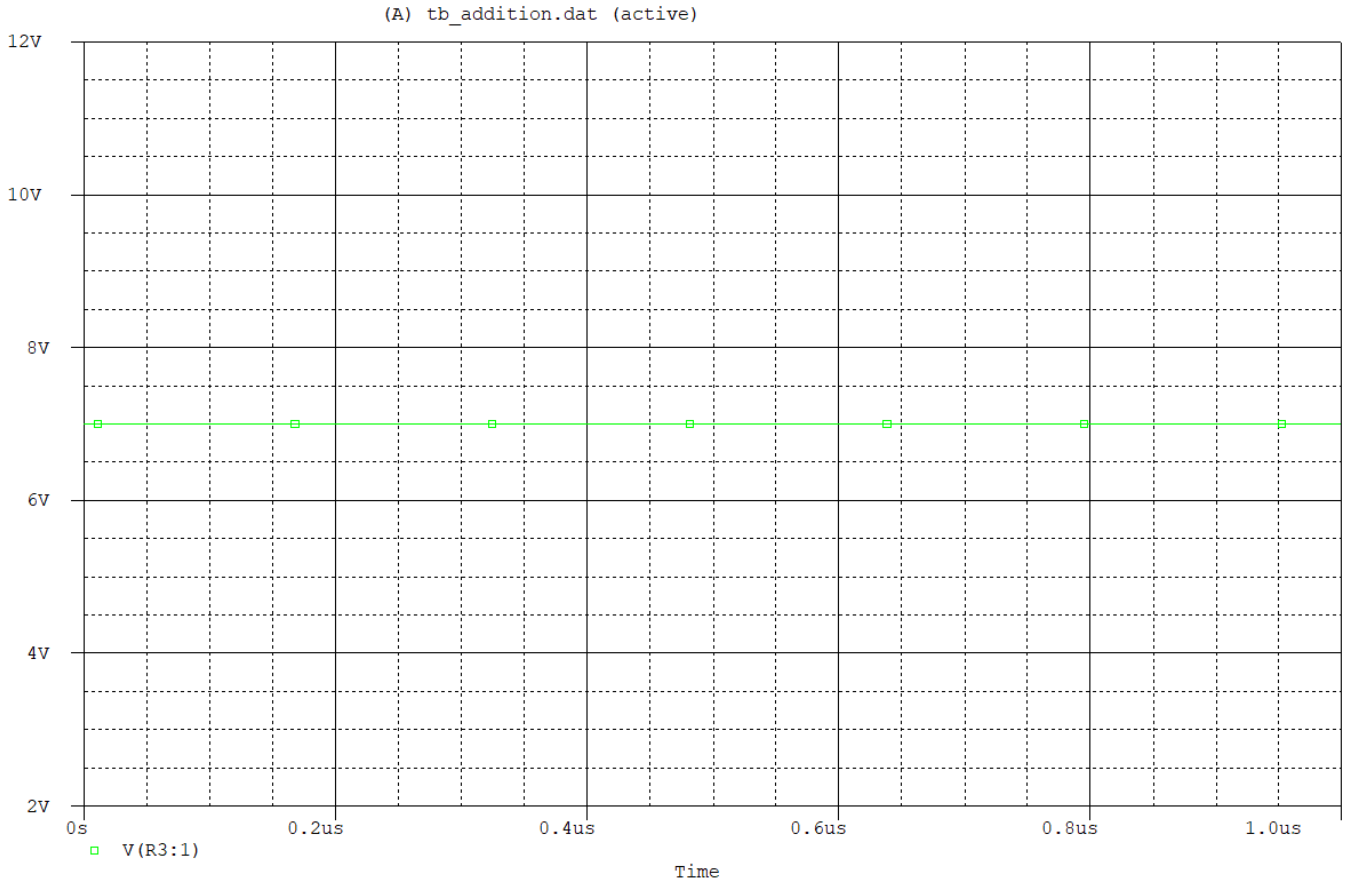


Figure 24. Pspice Simulation Result, Source: Adapted from [3]

Project Simulation (Cont.)

- Computer Simulation for each Circuit

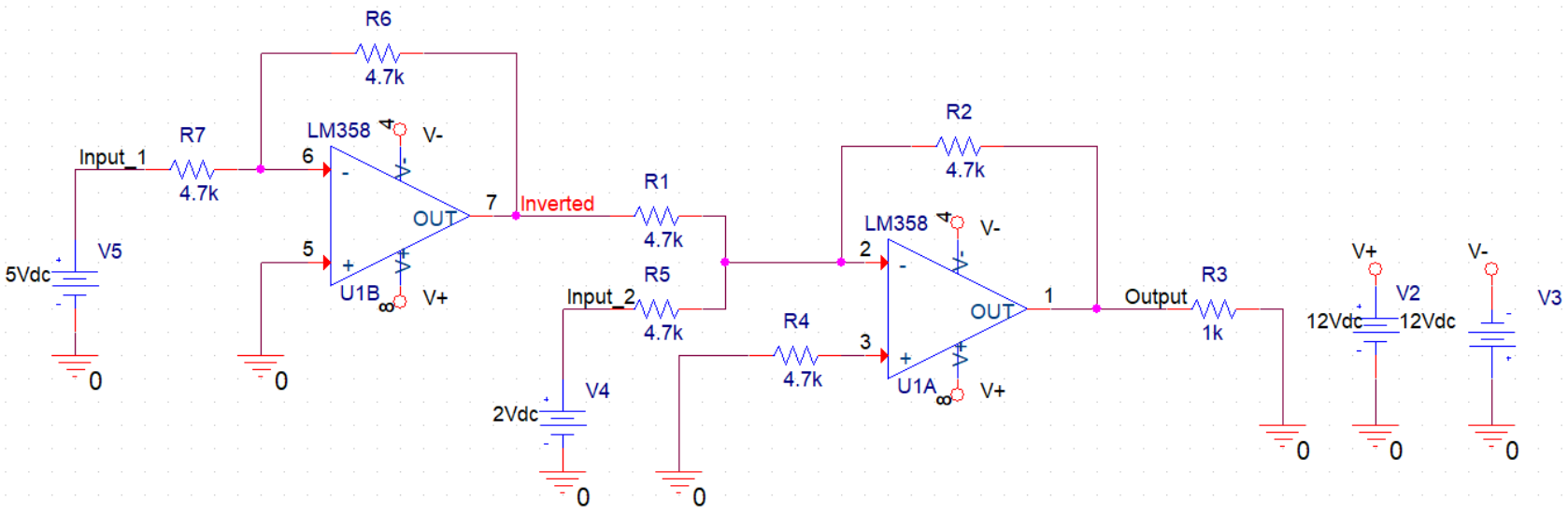


Figure 25. Pspice Subtraction Circuit Schematic , Source: Adapted from [3]

Project Simulation (Cont.)

- Computer Simulation for each Circuit

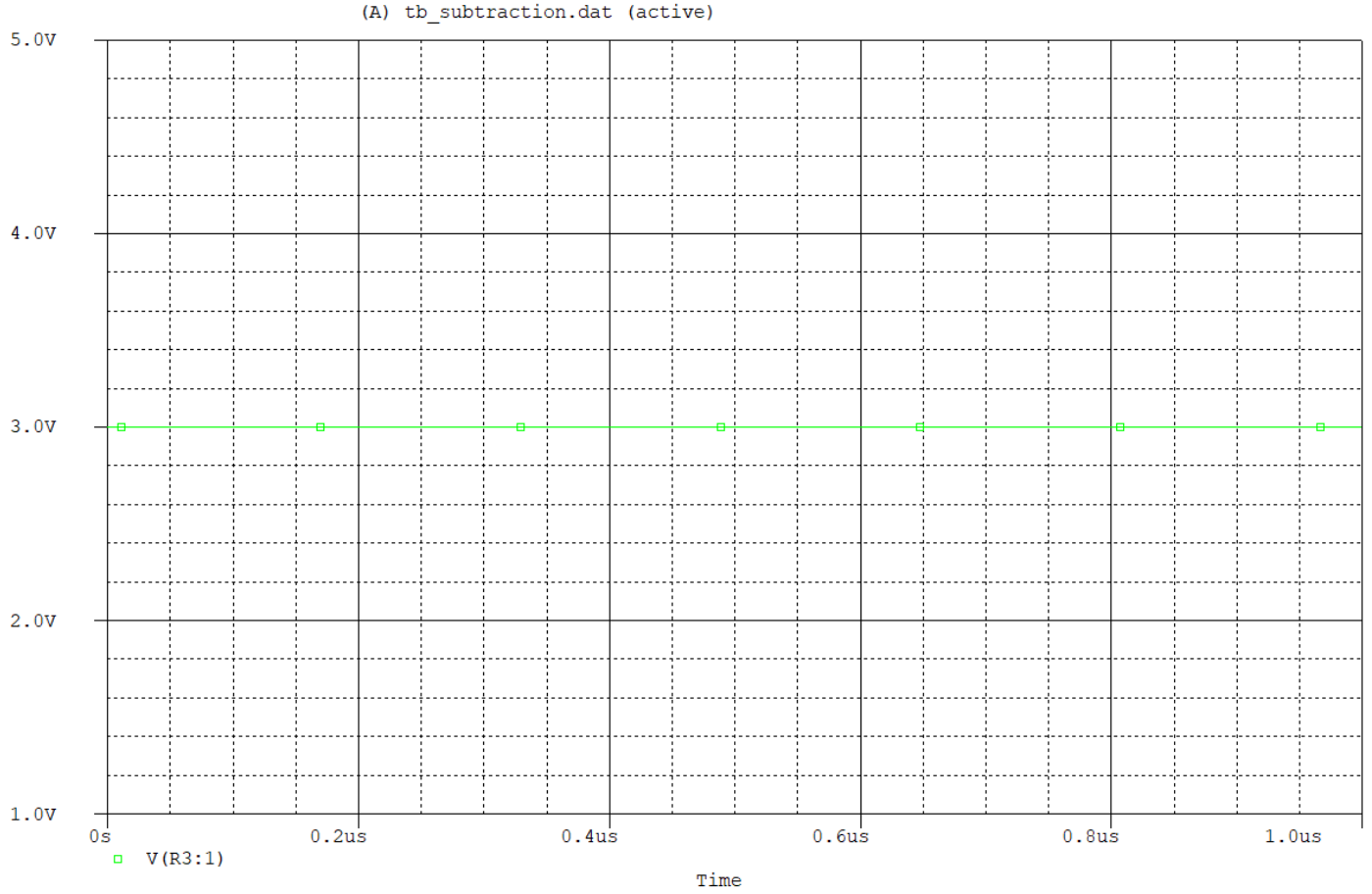


Figure 26. Pspice Simulation Result, Source: Adapted from [3]

Project Simulation (Cont.)

- Computer Simulation for each Circuit

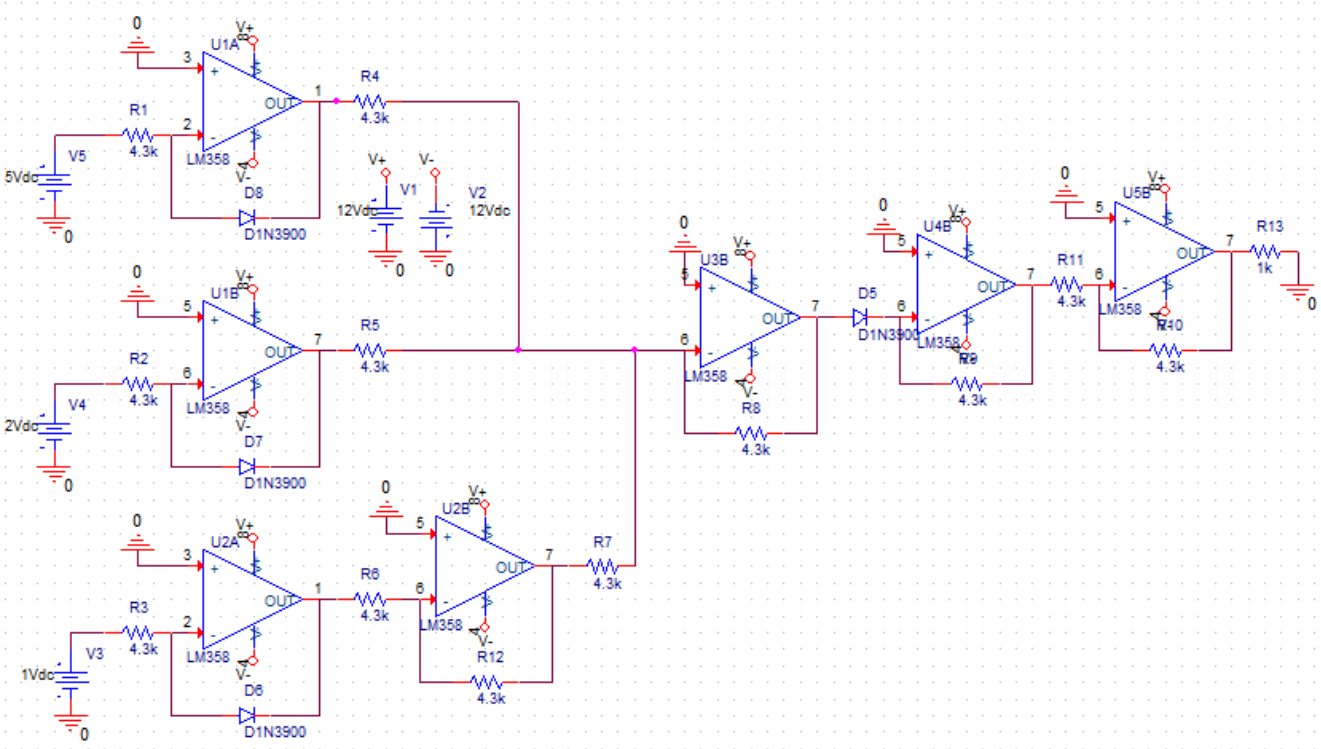


Figure 27. Pspice Multiplication Circuit Schematic , Source: Adapted from [3]

Project Simulation (Cont.)

- Computer Simulation for each Circuit

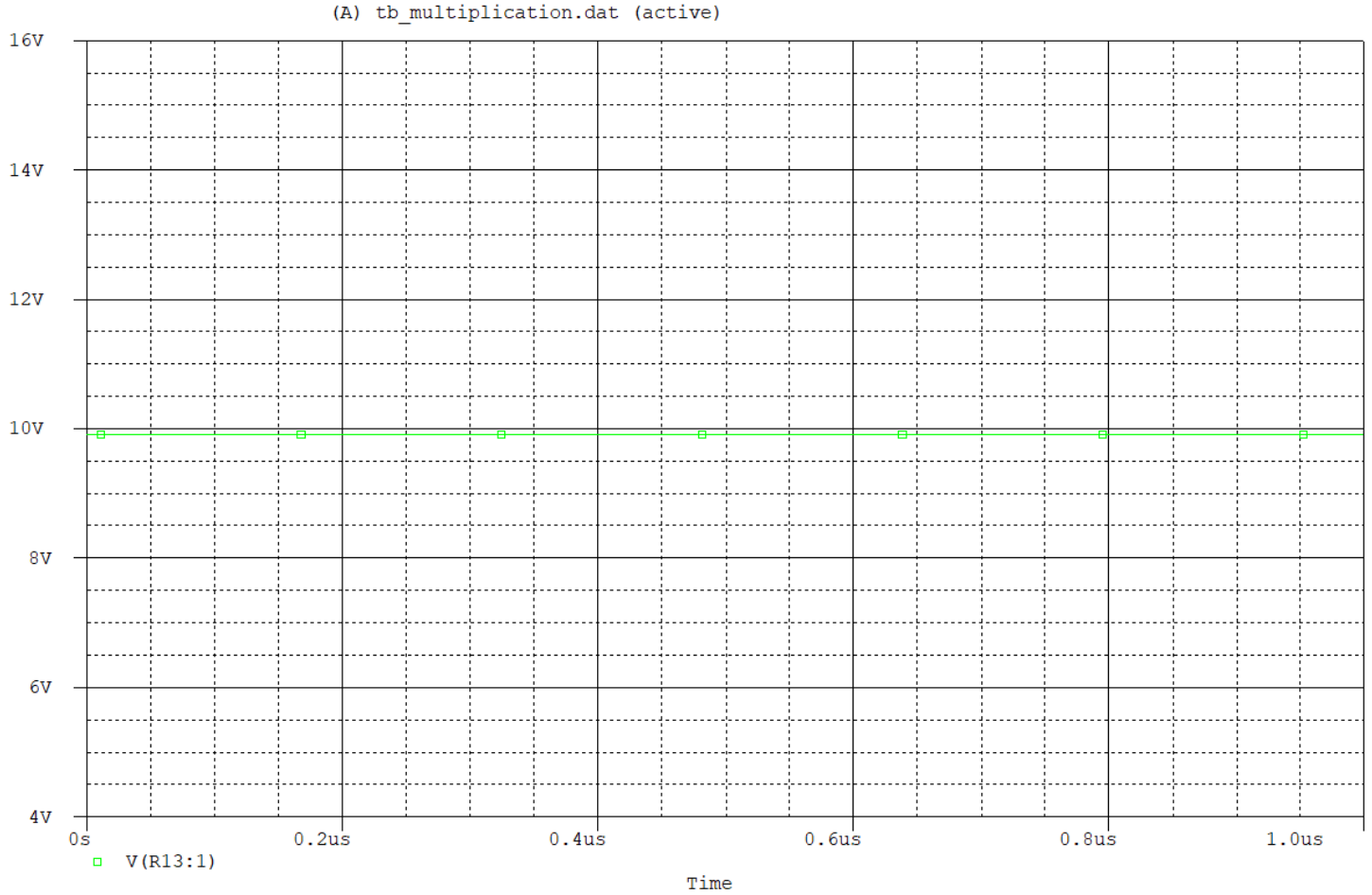


Figure 28. Pspice Simulation Result, Source: Adapted from [3]

Project Simulation (Cont.)

- Computer Simulation for each Circuit

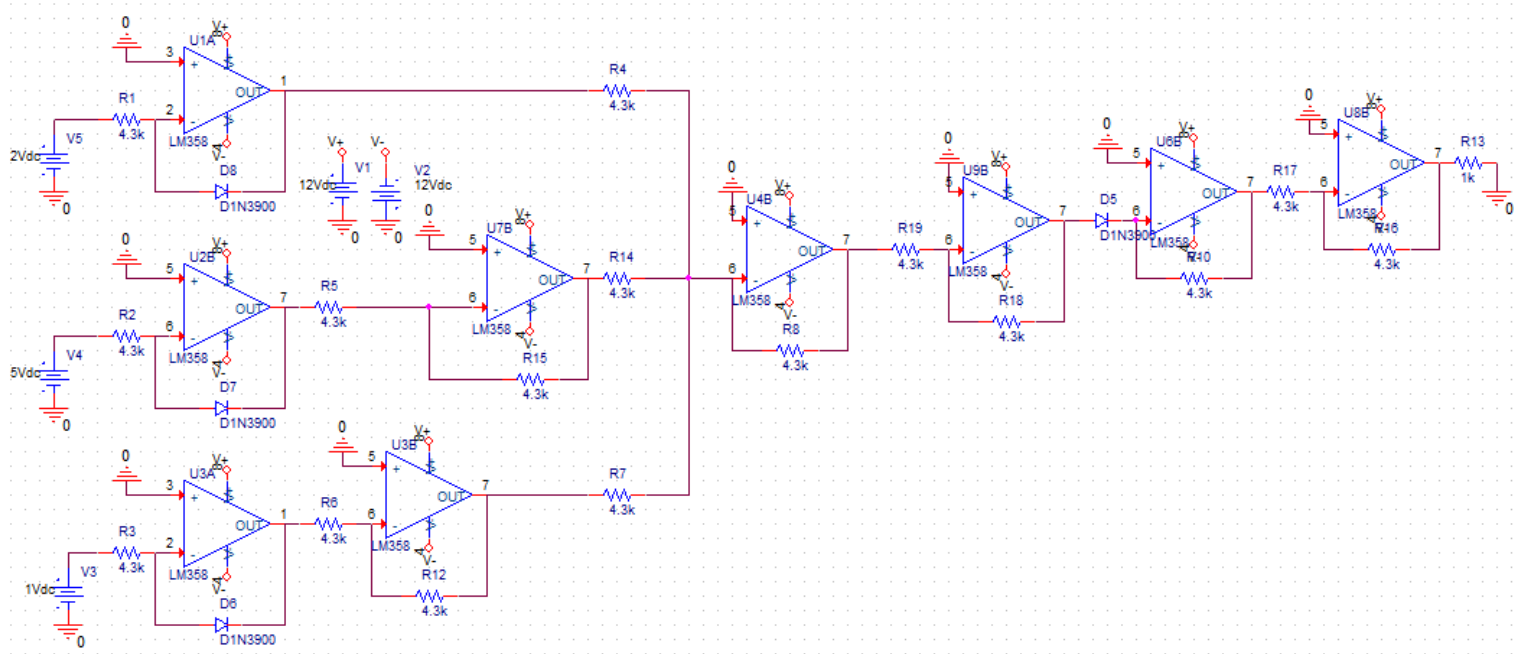


Figure 29. Pspice Division Circuit Schematic , Source: Adapted from [3]

Project Simulation (Cont.)

- Computer Simulation for each Circuit

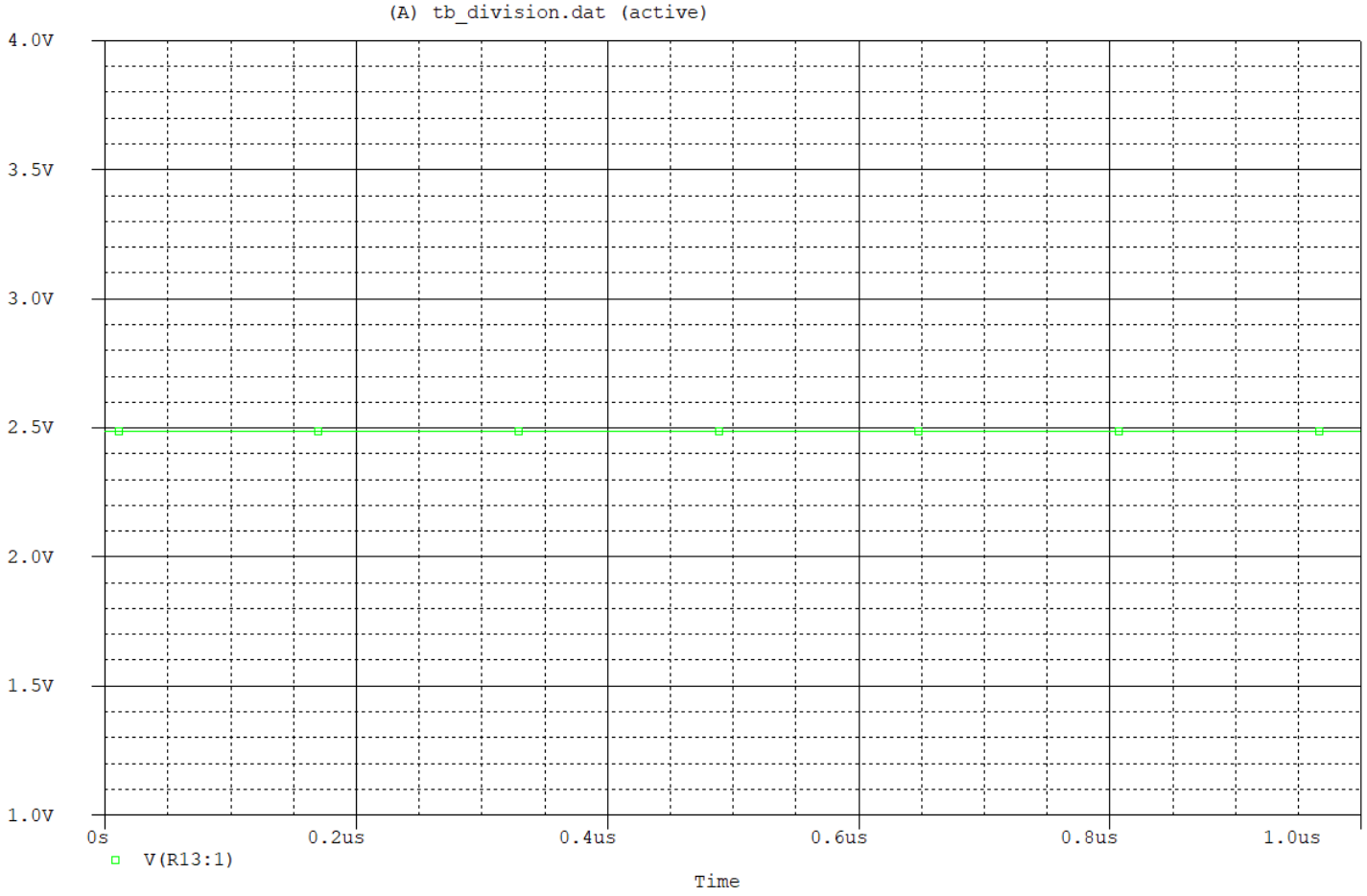


Figure 30. Pspice Simulation Result, Source: Adapted from [3]

Project Simulation (Cont.)

- Computer Simulation for the Power Supply

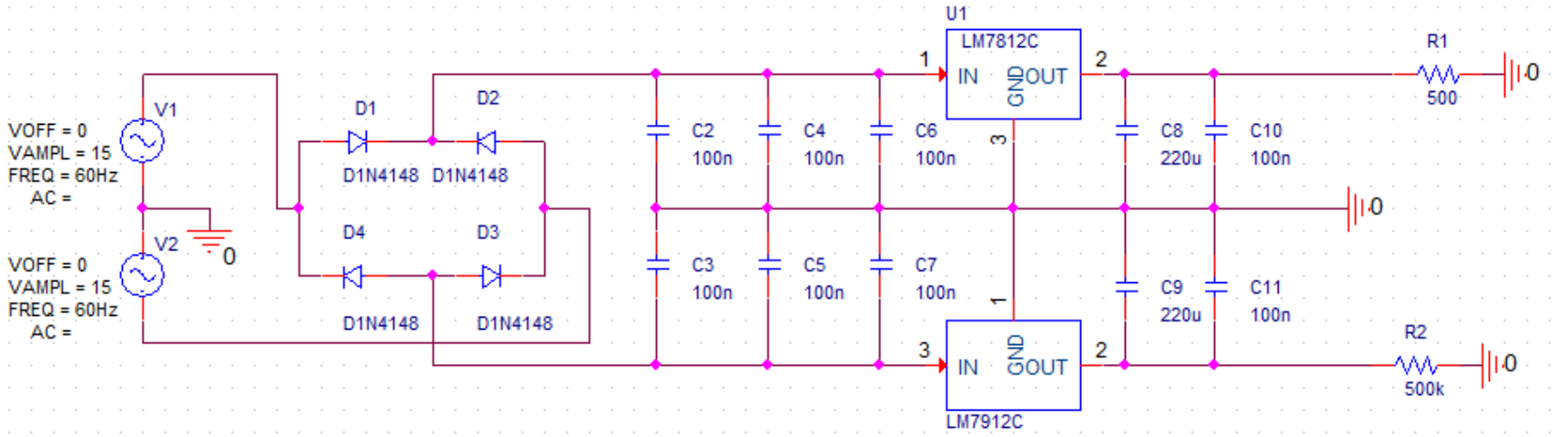
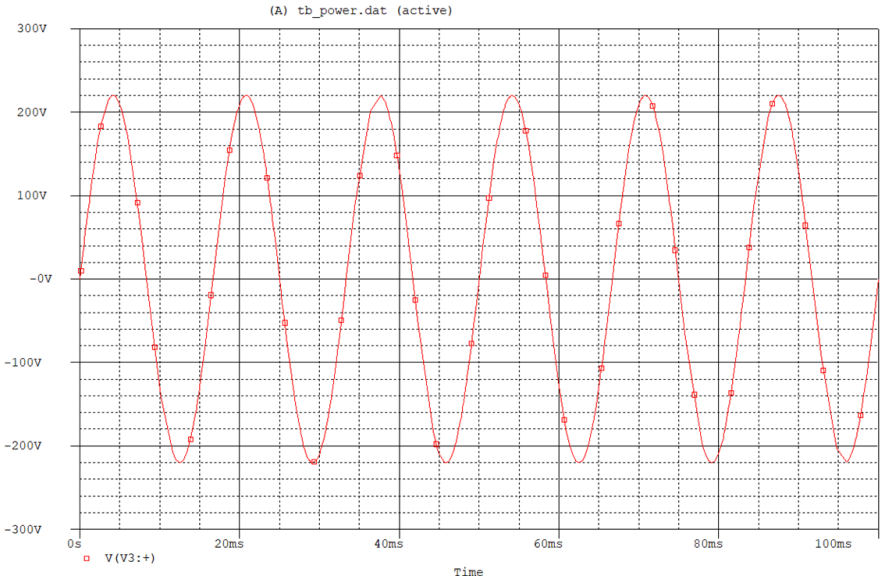


Figure 31. Pspice Power Supply Circuit Schematic, Source: Adapted from [3]

Project Simulation (Cont.)

- Computer Simulation for the Power Supply



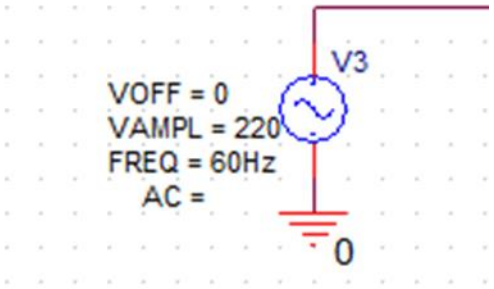
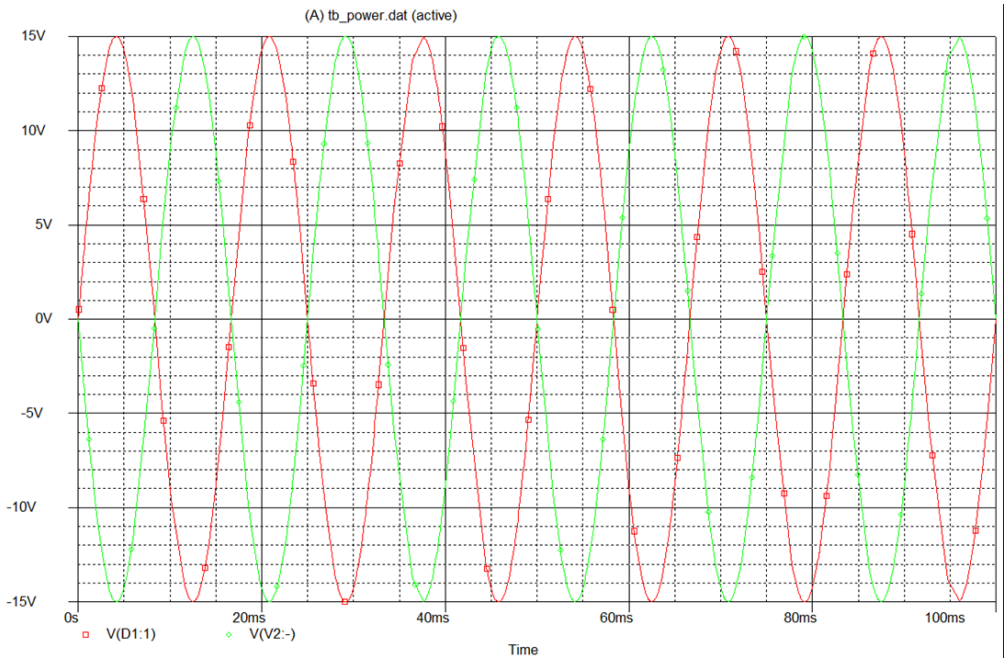


Figure 32. Pspice Simulation Result (Power Supply Input Voltage of 220V AC @ 60Hz), Source: Adapted from [3]

Project Simulation (Cont.)

- Computer Simulation for the Power Supply



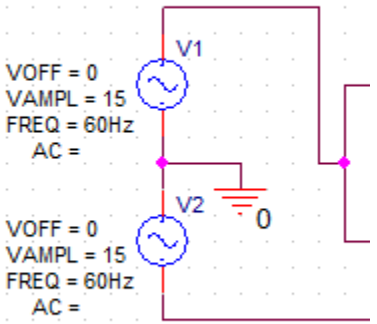


Figure 33. Pspice Simulation Result (Power Supply Input Voltage After passing the Transformer), Source: Adapted from [3]

Project Simulation (Cont.)

- Computer Simulation for the Power Supply

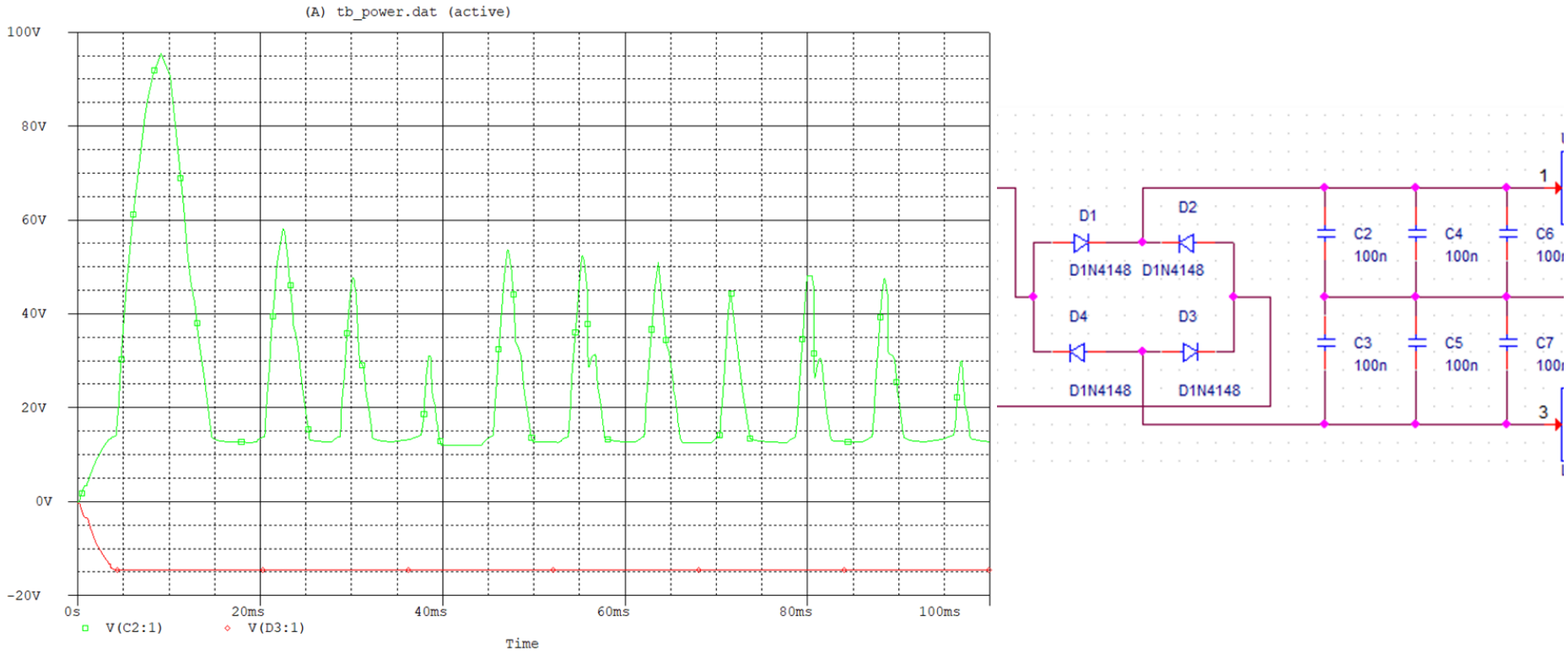
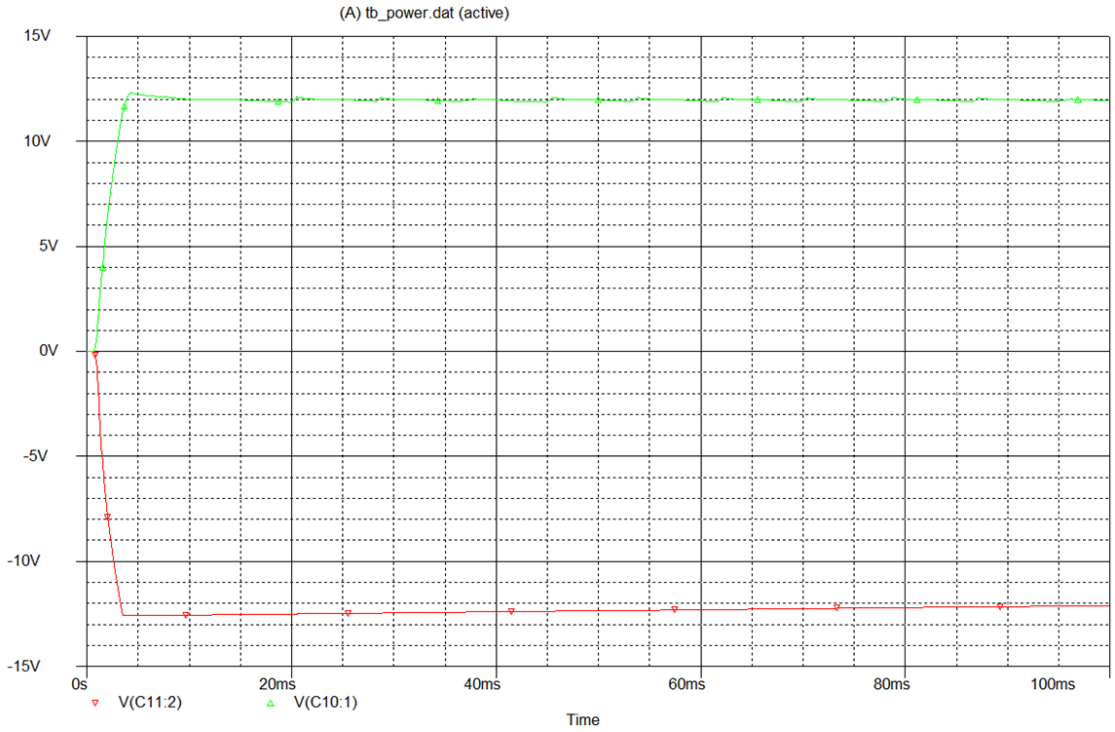


Figure 34. Pspice Simulation Result (Power Supply Input Voltage After passing the Bridge Diode), Source: Adapted from [3]

Project Simulation (Cont.)

- Computer Simulation for the Power Supply



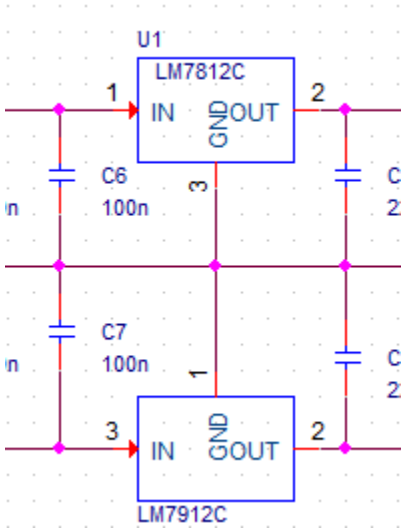
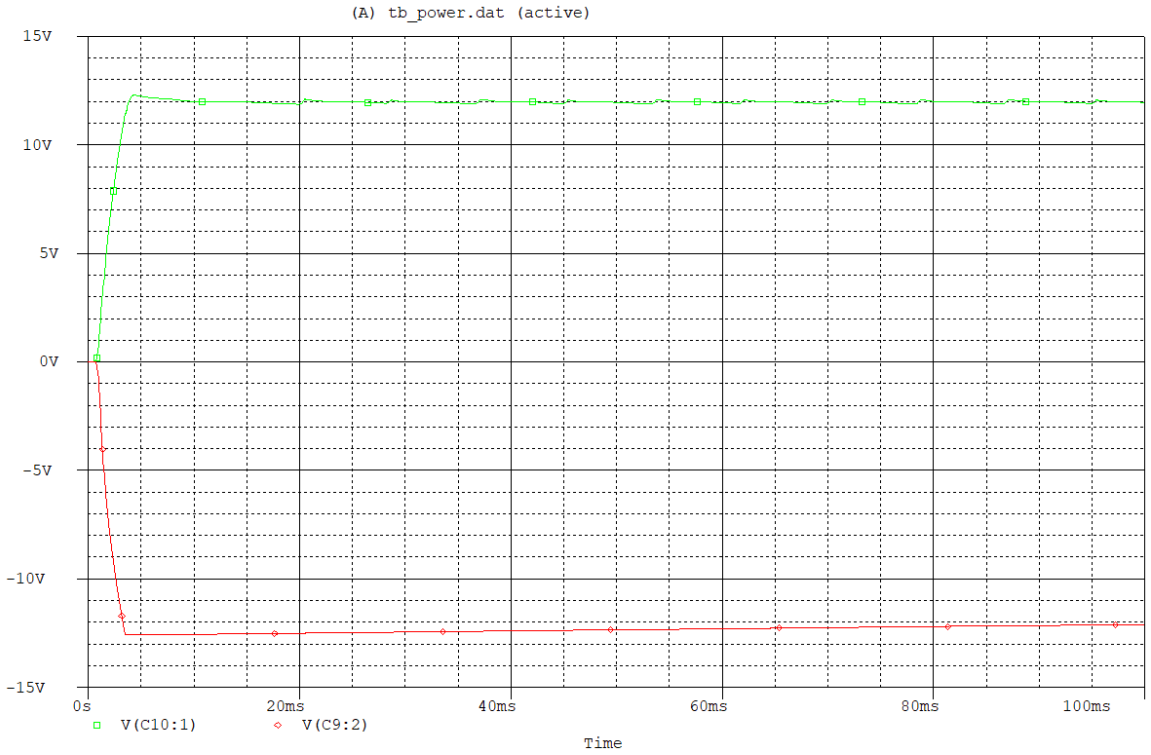


Figure 35. Pspice Simulation Result (Power Supply Input Voltage After passing the Regulators), Source: Adapted from [3]

Project Simulation (Cont.)

- Computer Simulation for the Power Supply



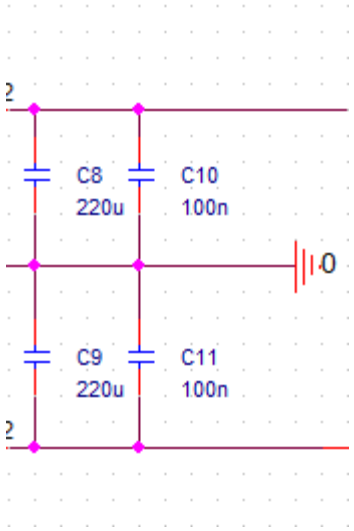


Figure 36. Pspice Simulation Result (Power Supply outputting +12 and -12 from AC 220V), Source: Adapted from [3]

Project Simulation (Cont.)

- Breadboard Testing

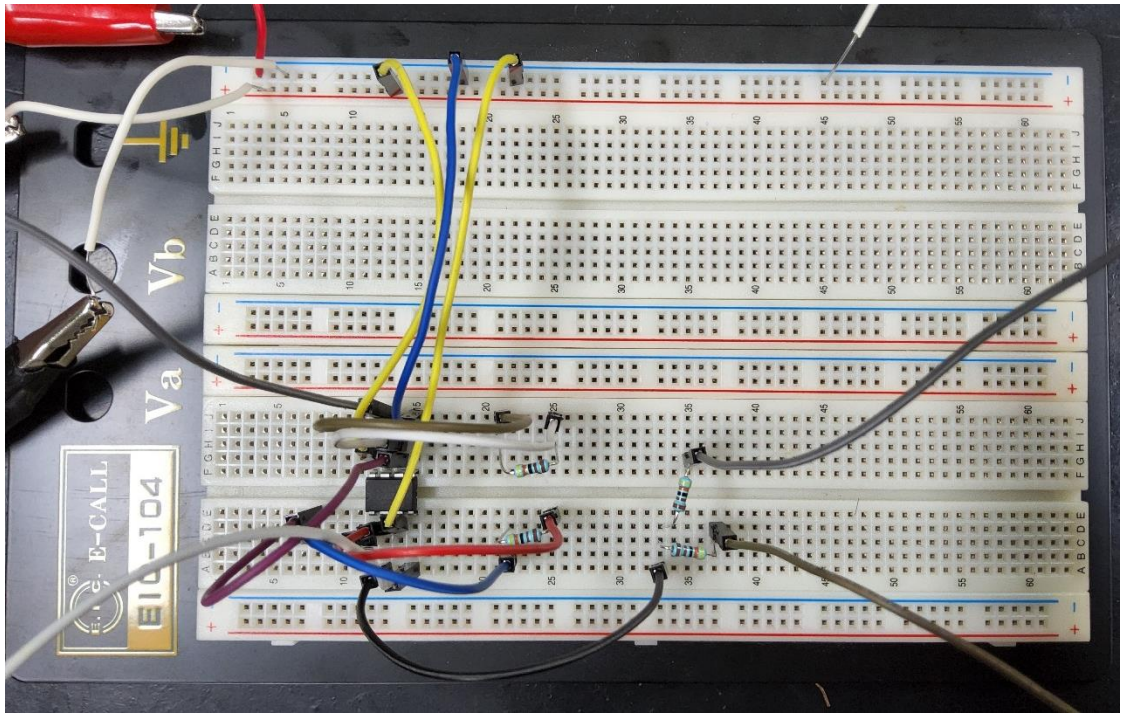


Figure 37. Addition Module Testing on Breadboard

Project Simulation (Cont.)

- Breadboard Testing

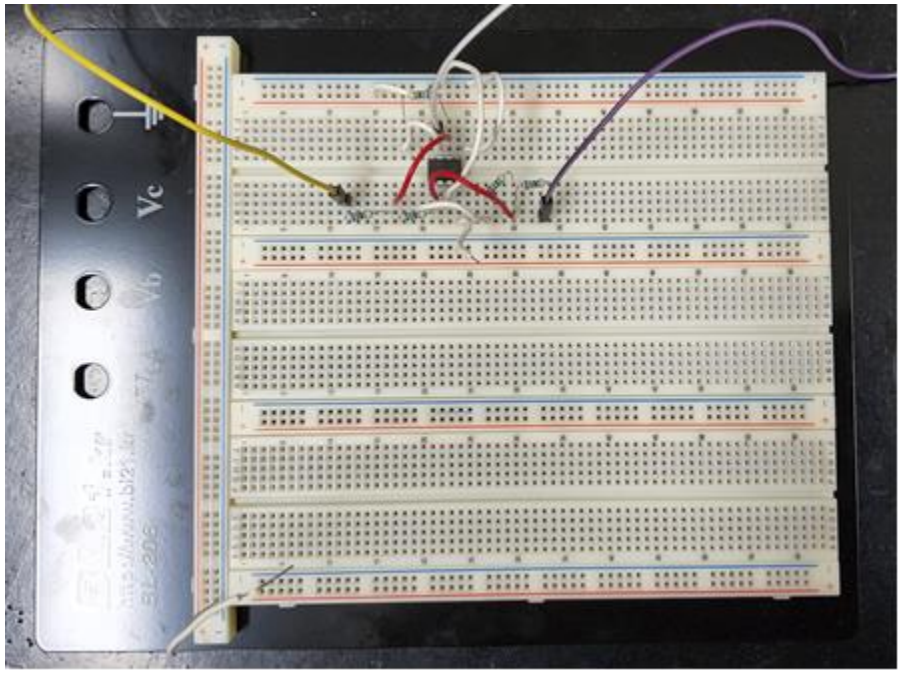


Figure 38. Subtraction Module Testing on Breadboard

Project Simulation (Cont.)

- Breadboard Testing

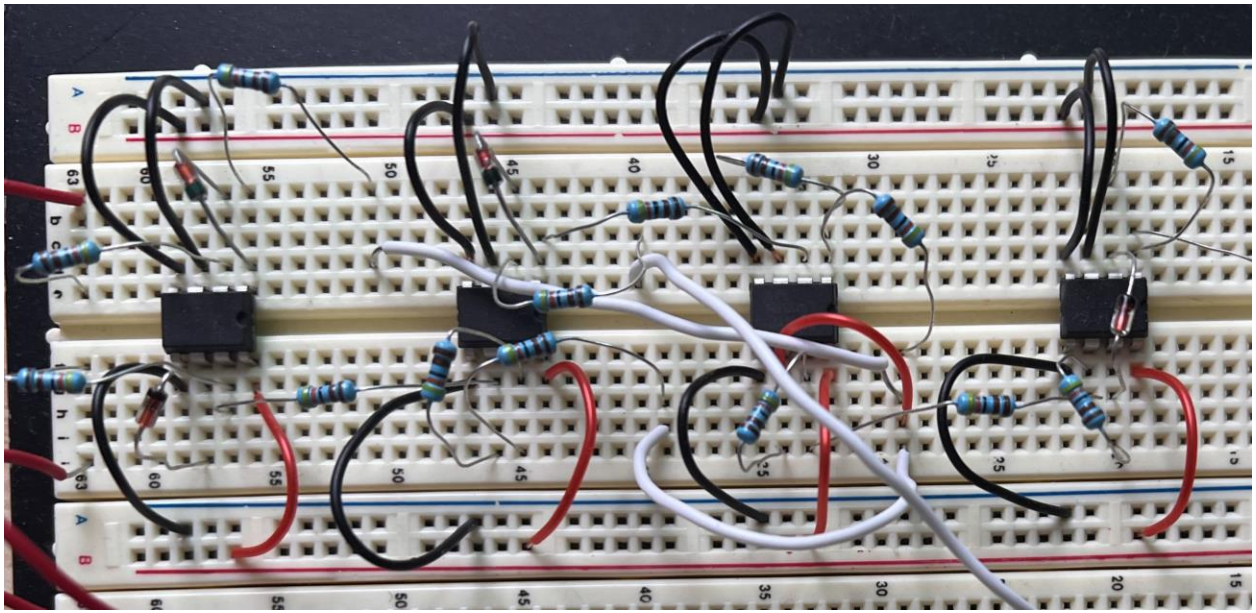


Figure 39. Multiplication Module Testing on Breadboard

Project Simulation (Cont.)

- Breadboard Testing

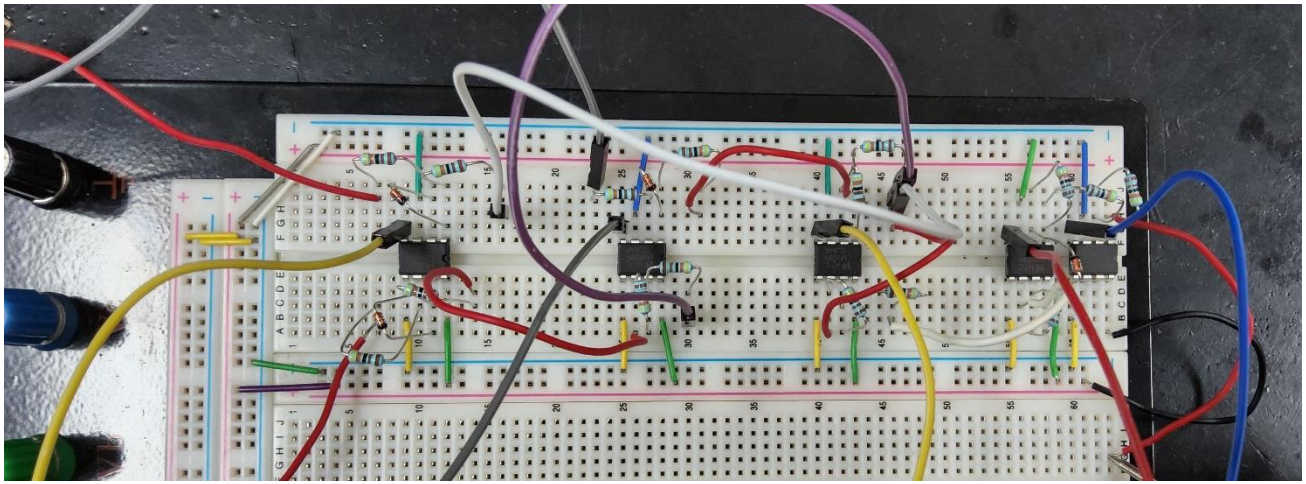


Figure 40. Division Module Testing on Breadboard

Project Simulation (Cont.)

- Breadboard Testing

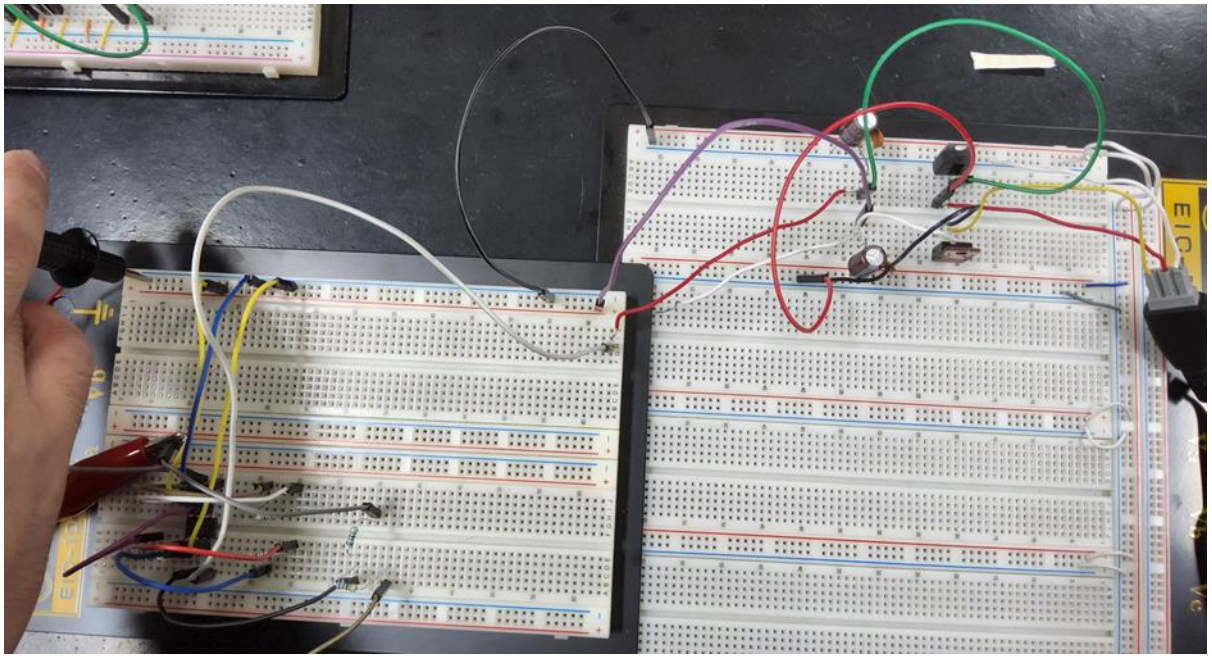


Figure 41. Power Supply and Addition Module Integration Test (Left) and Result (Right)

Project Simulation (Cont.)

- Voltage Control Test On Breadboard

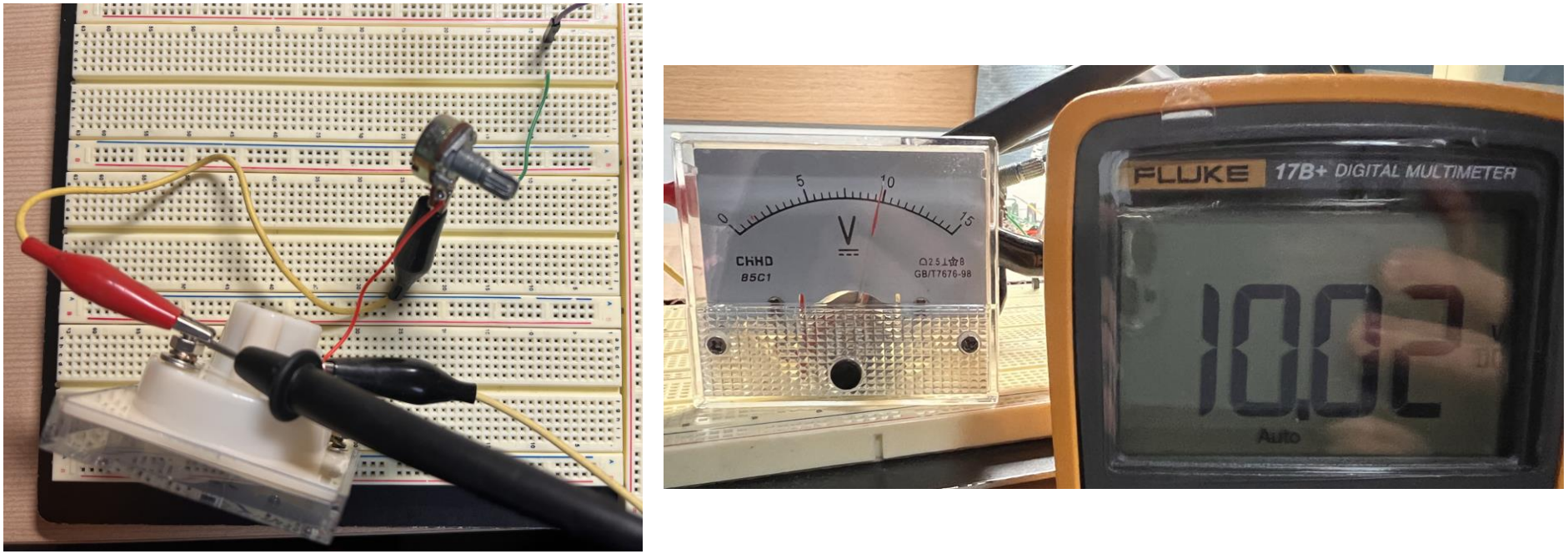
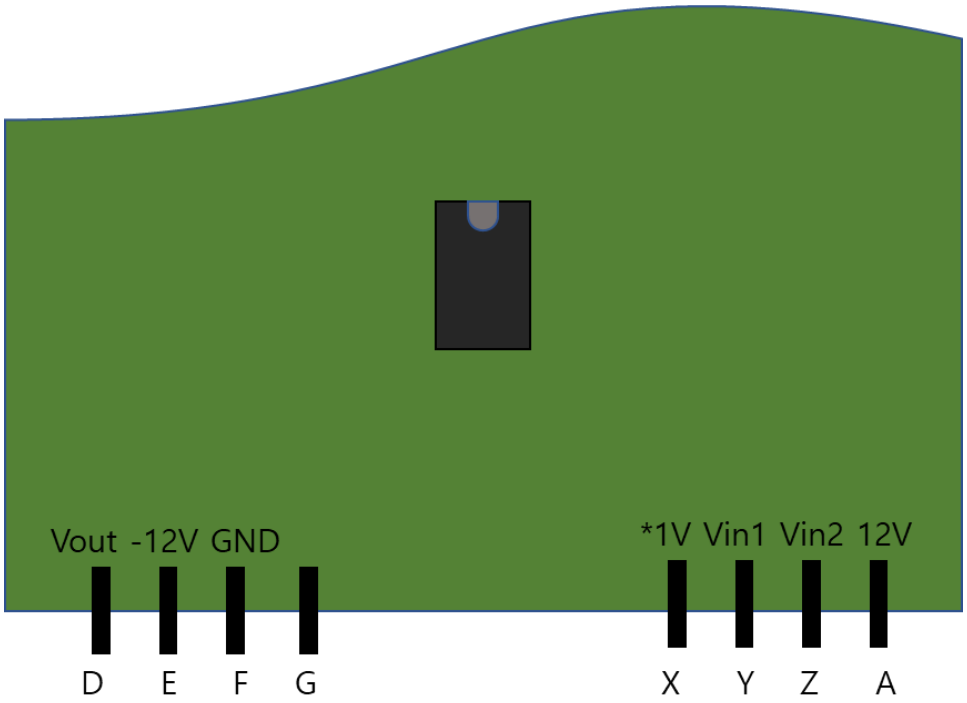


Figure 42. Voltage Control Test with Potentiometer and Voltmeter Connected (Left) and Result (Right)

- Use 10K Ohms potentiometer to prevent high currents from passing.

CHAPTER 2 : DEVELOPMENT OF PRODUCT

Soldering Modules



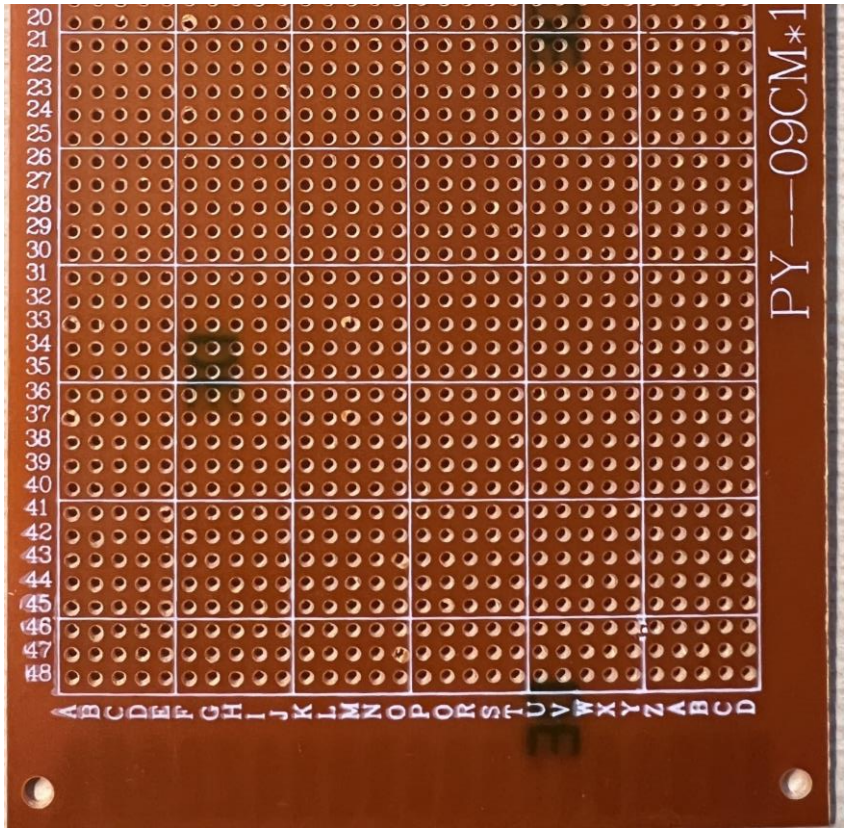
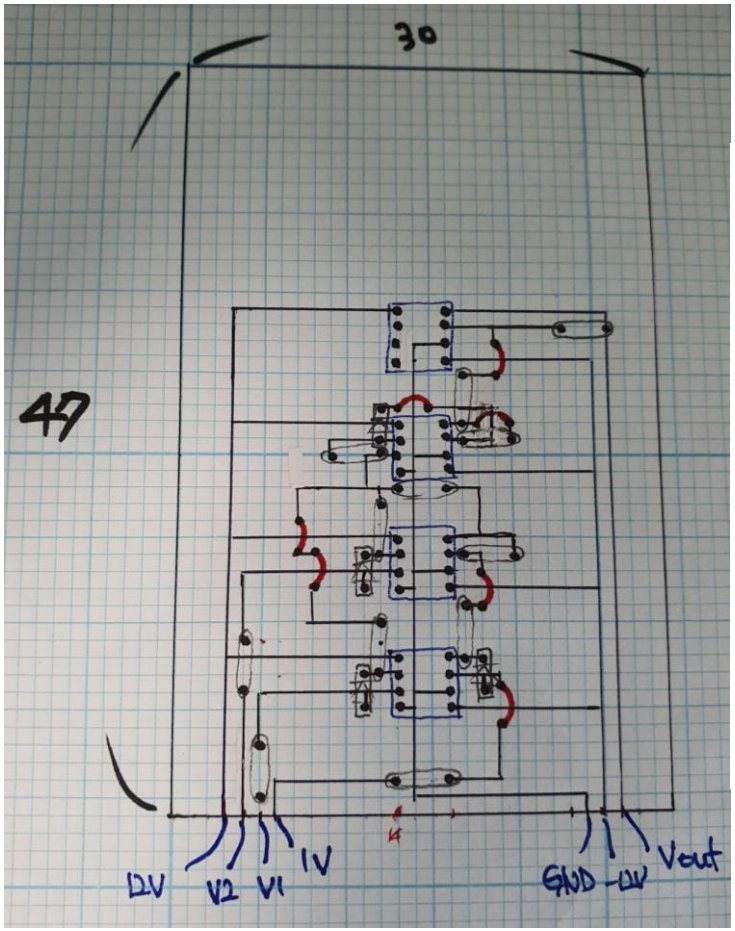


Figure 43. Pin Configuration for Each Module (Left) Perfboard Pin Reference (Right), Source: Made with PowerPoint

Soldering Modules (Cont.)



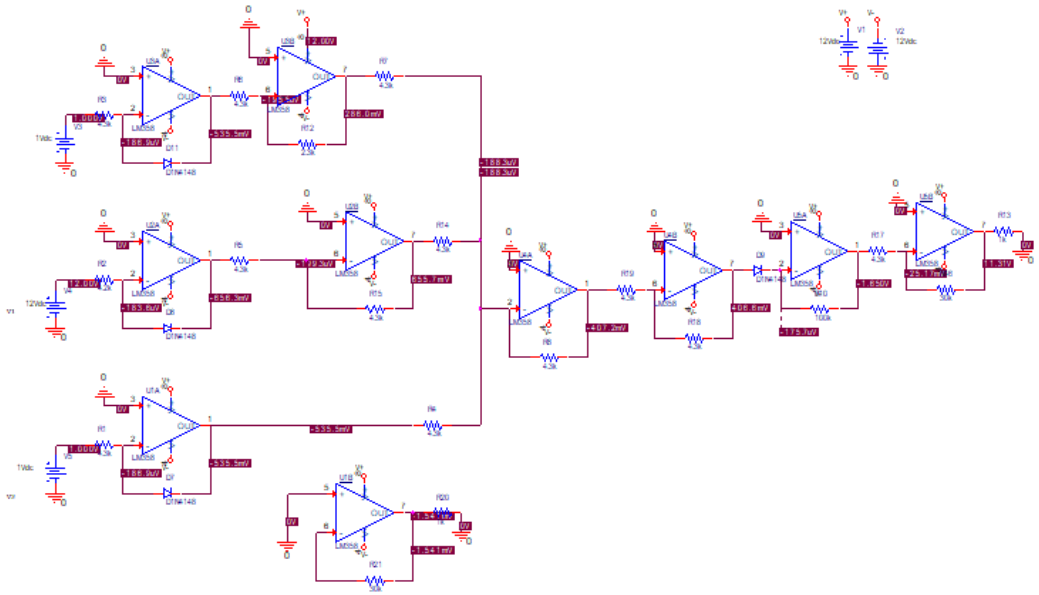


Figure 44. Schematics for each for Multiplication and Division Module, Source: Adapted from [3]

Soldering Modules (Cont.)

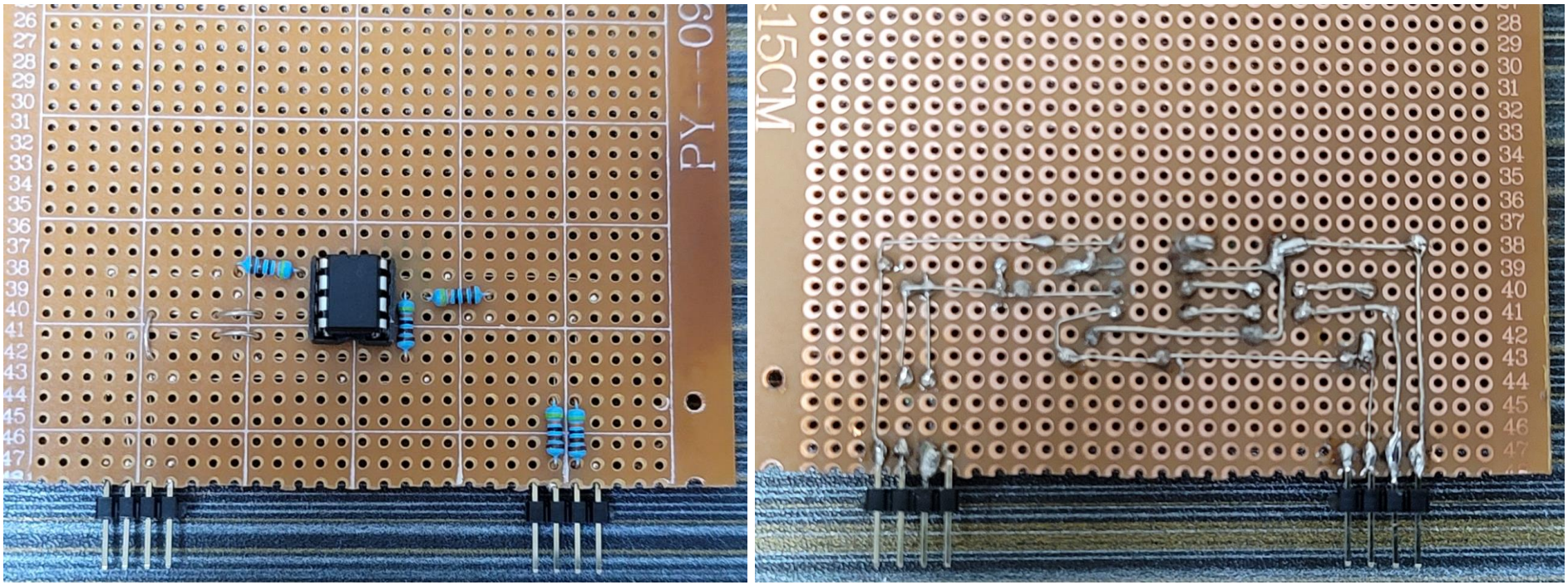


Figure 45. Addition Module

Soldering Modules (Cont.)

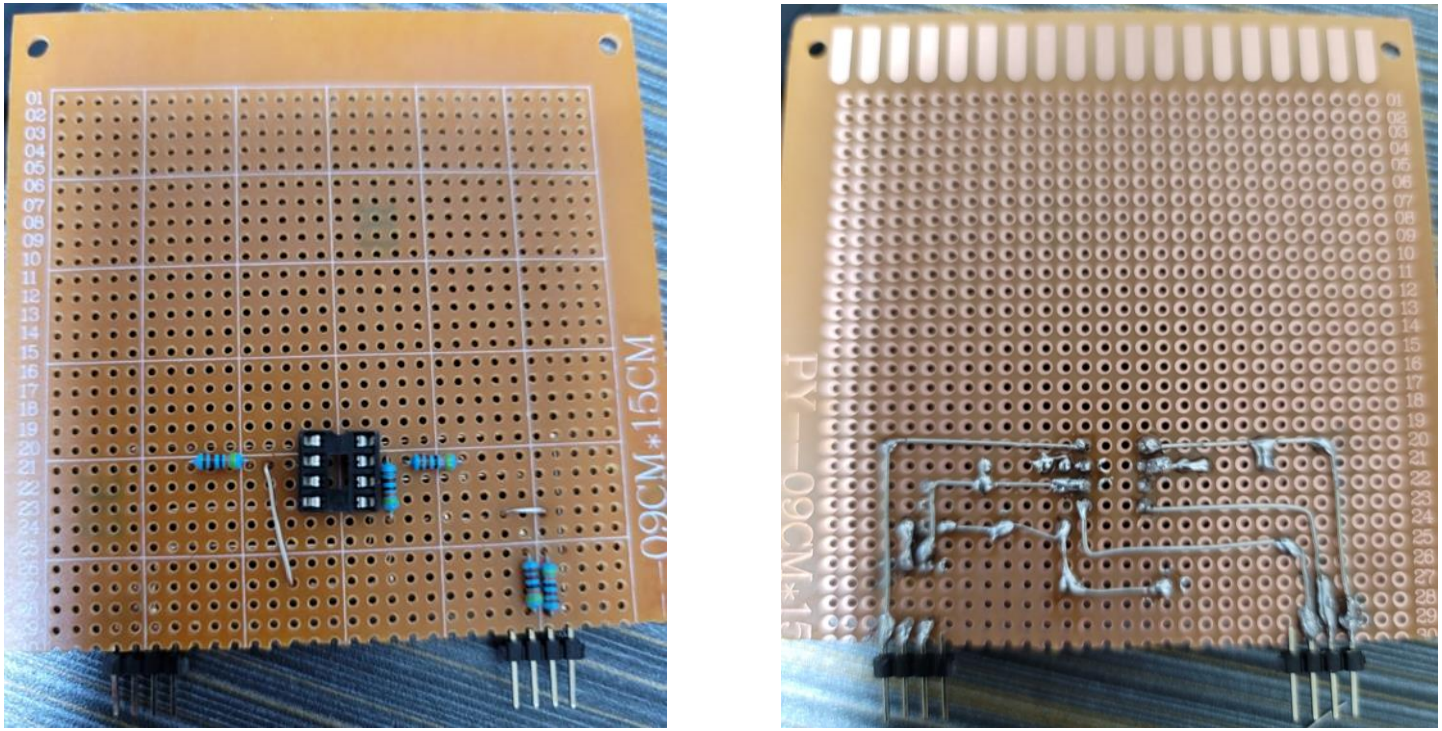


Figure 46. Subtraction Module

Soldering Modules (Cont.)

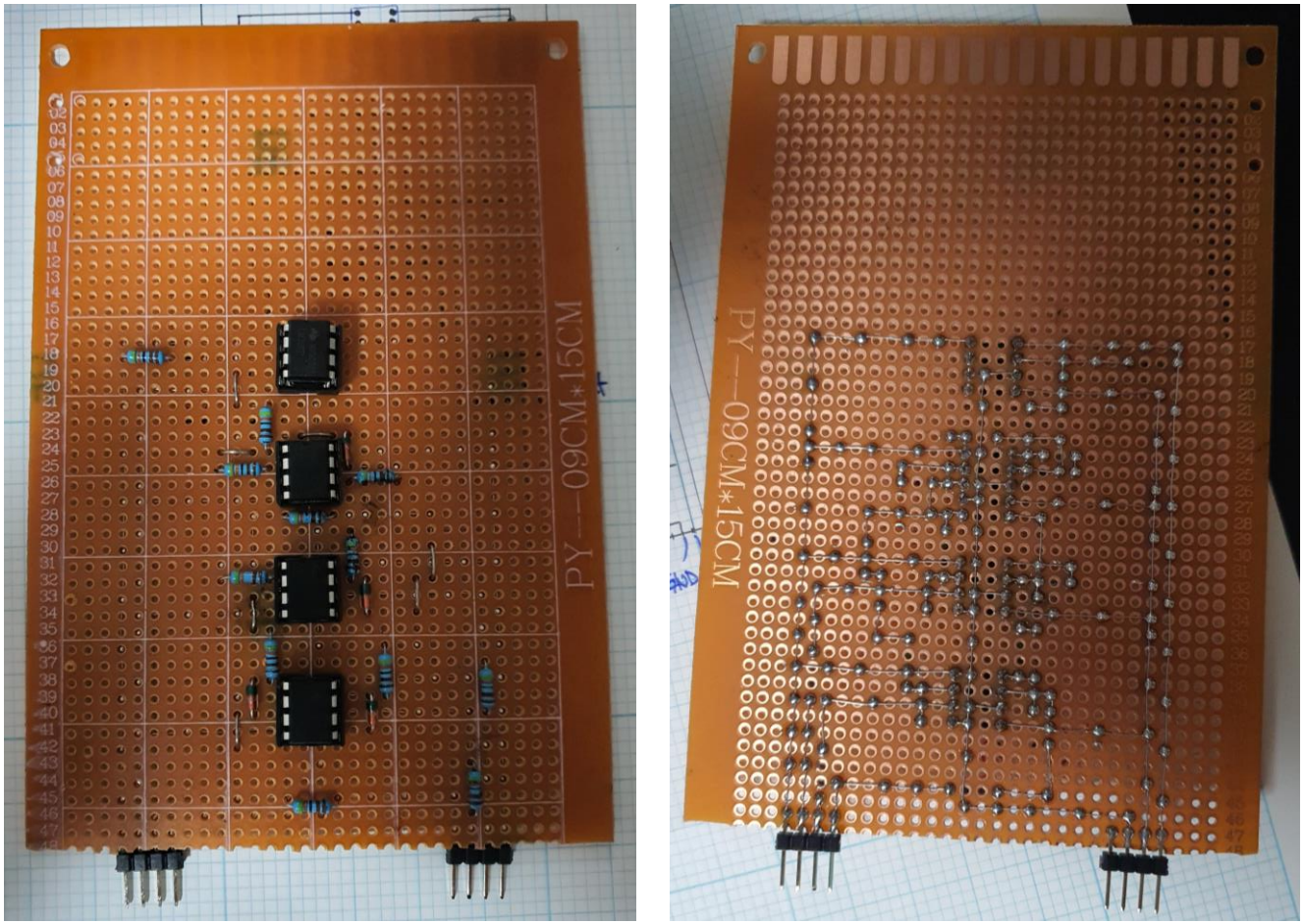


Figure 47. Multiplication Module

Soldering Modules (Cont.)

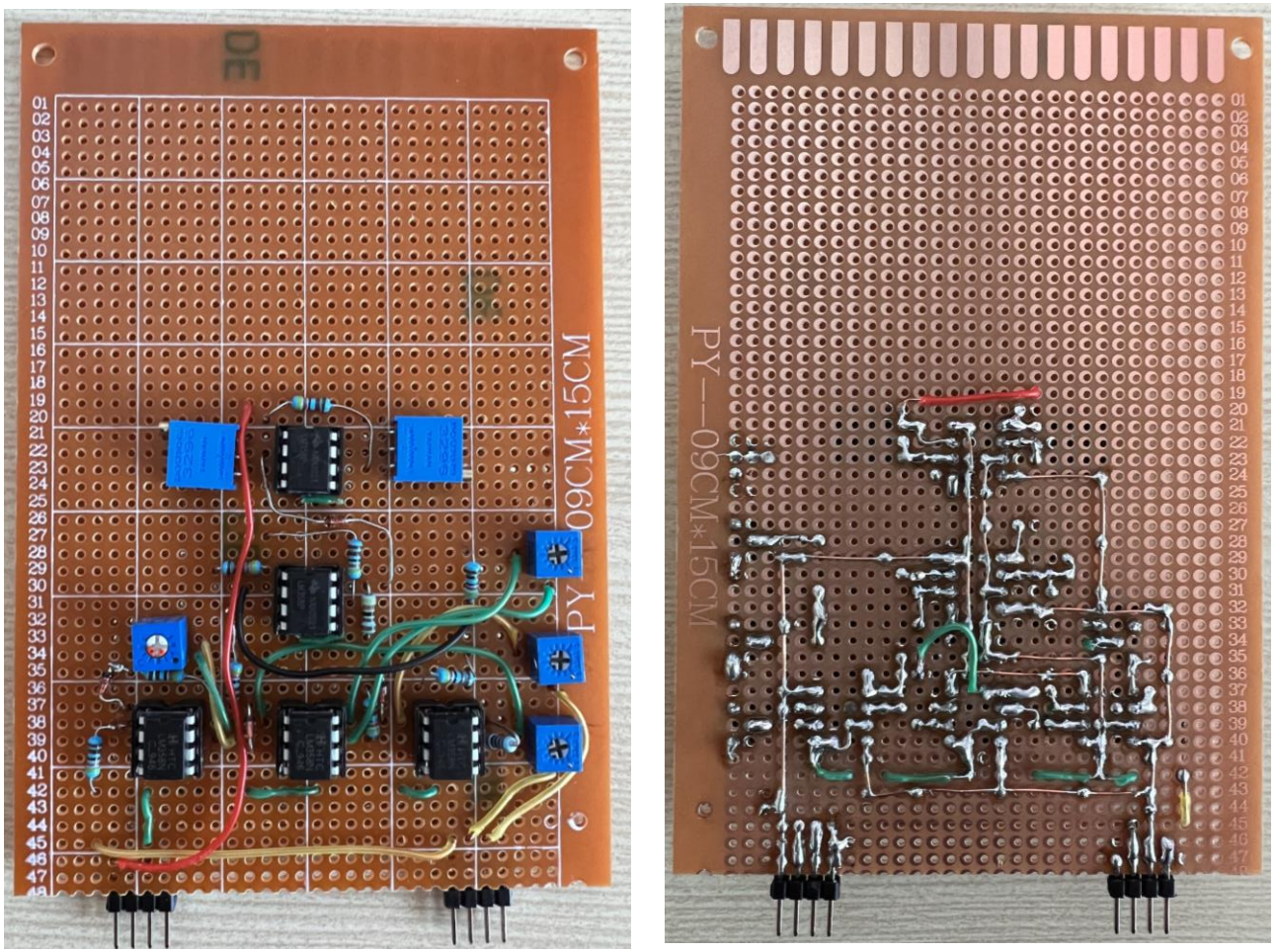


Figure 48. Division Module

Soldering Modules (Cont.)

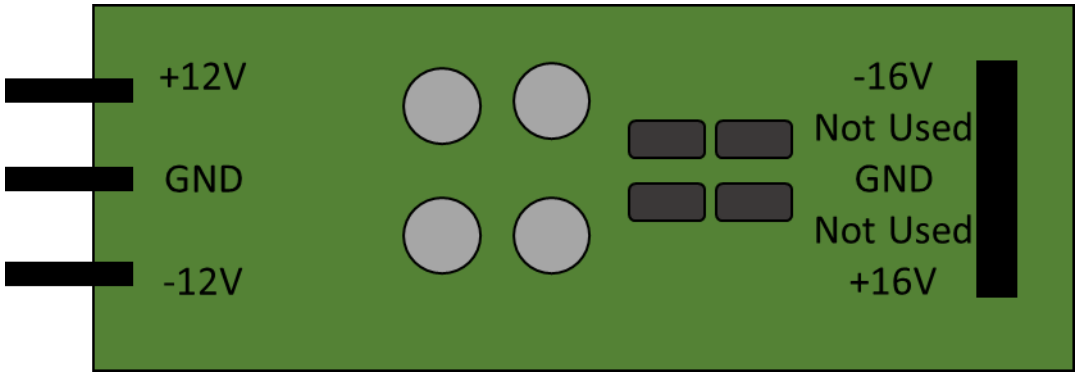


Figure 49. Power Supply Module Pin Configuration, Source: Made with PowerPoint

Testing Modules

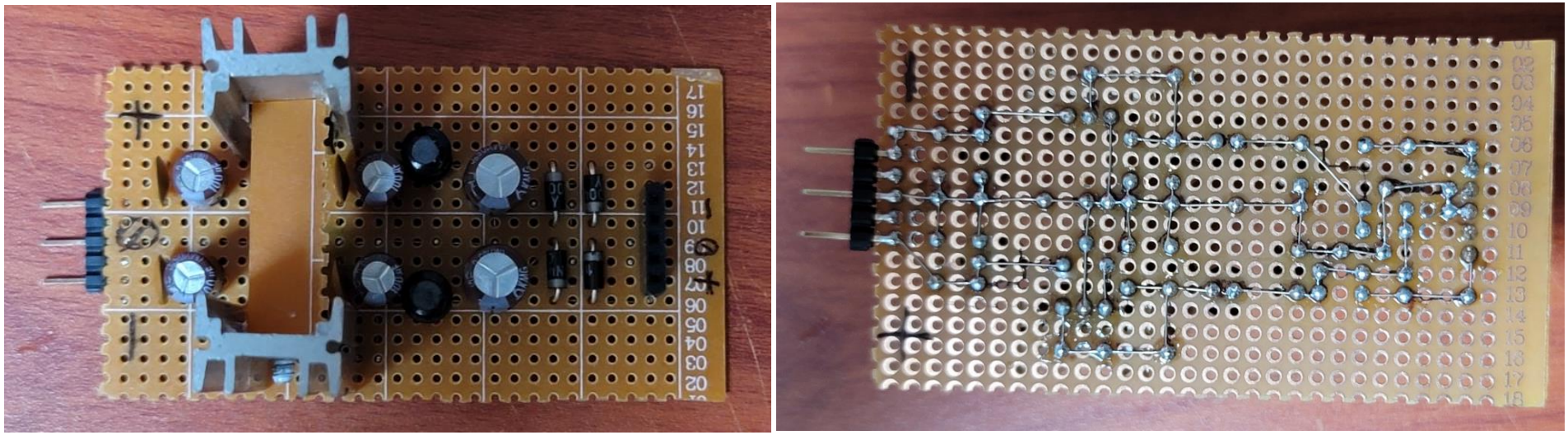


Figure 50. Power Supply Module

Testing Modules (Cont.)

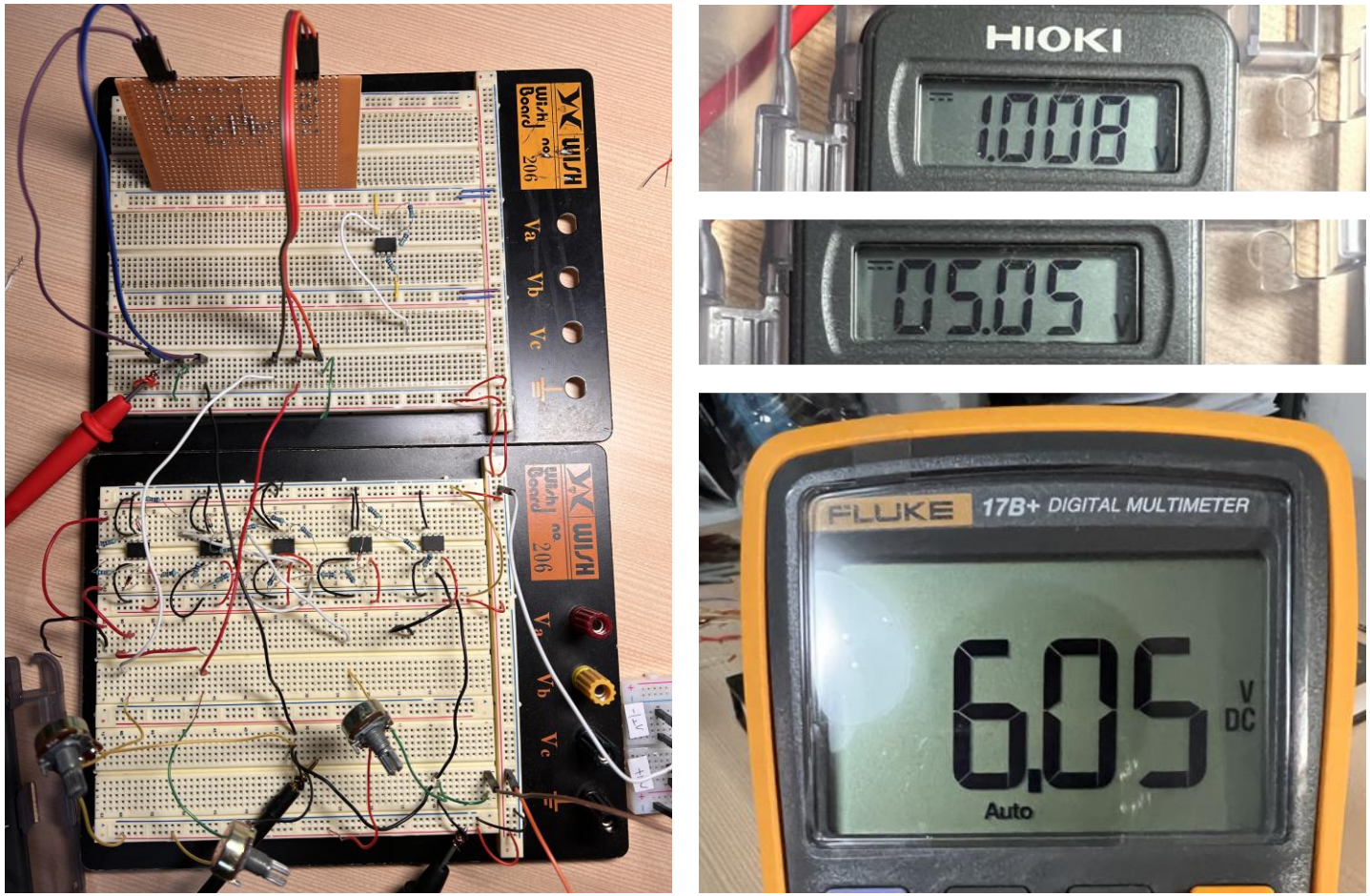


Figure 51. Testing Addition Module

Testing Modules (Cont.)

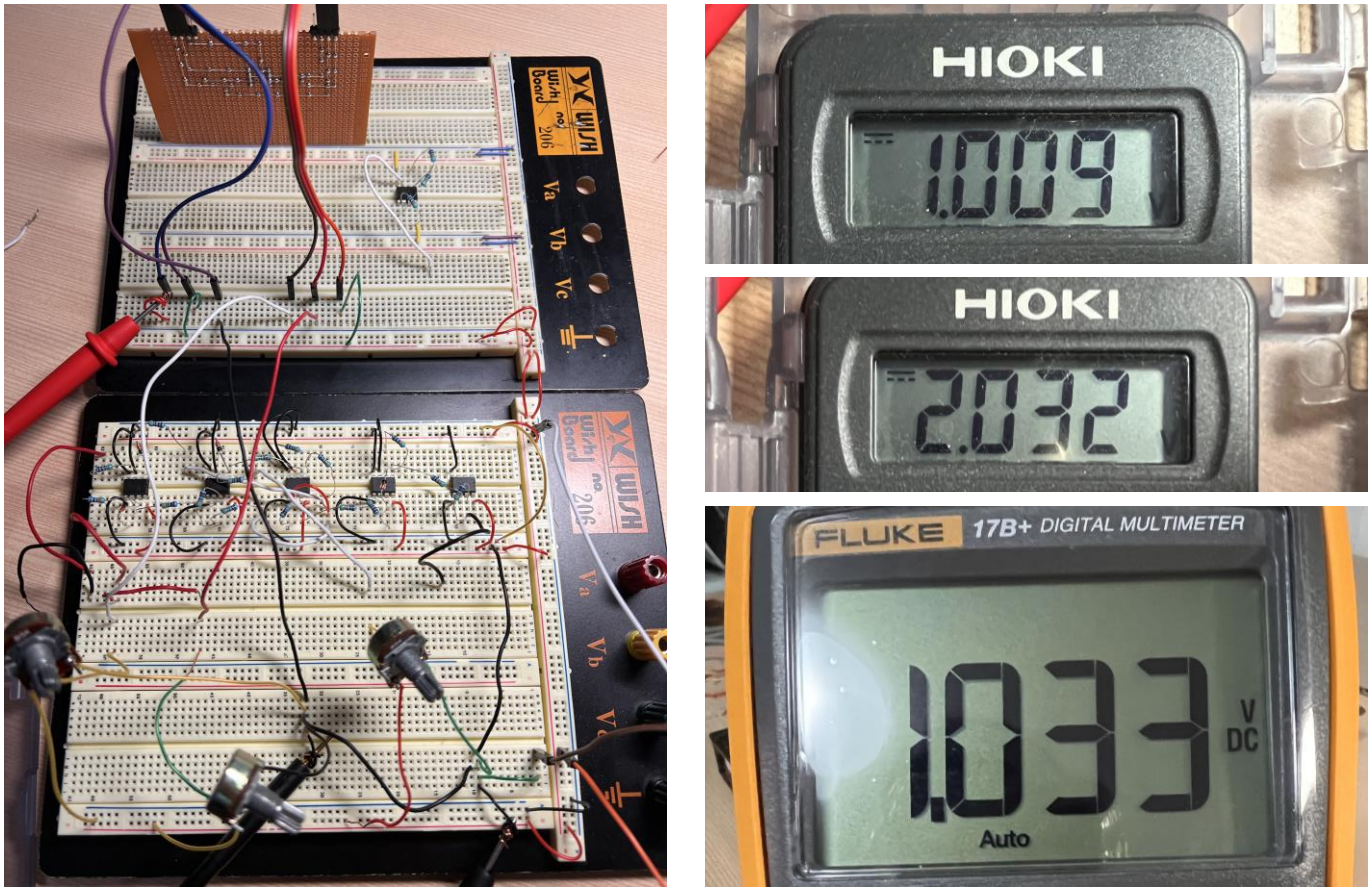


Figure 52. Testing Subtraction Module

Testing Modules (Cont.)

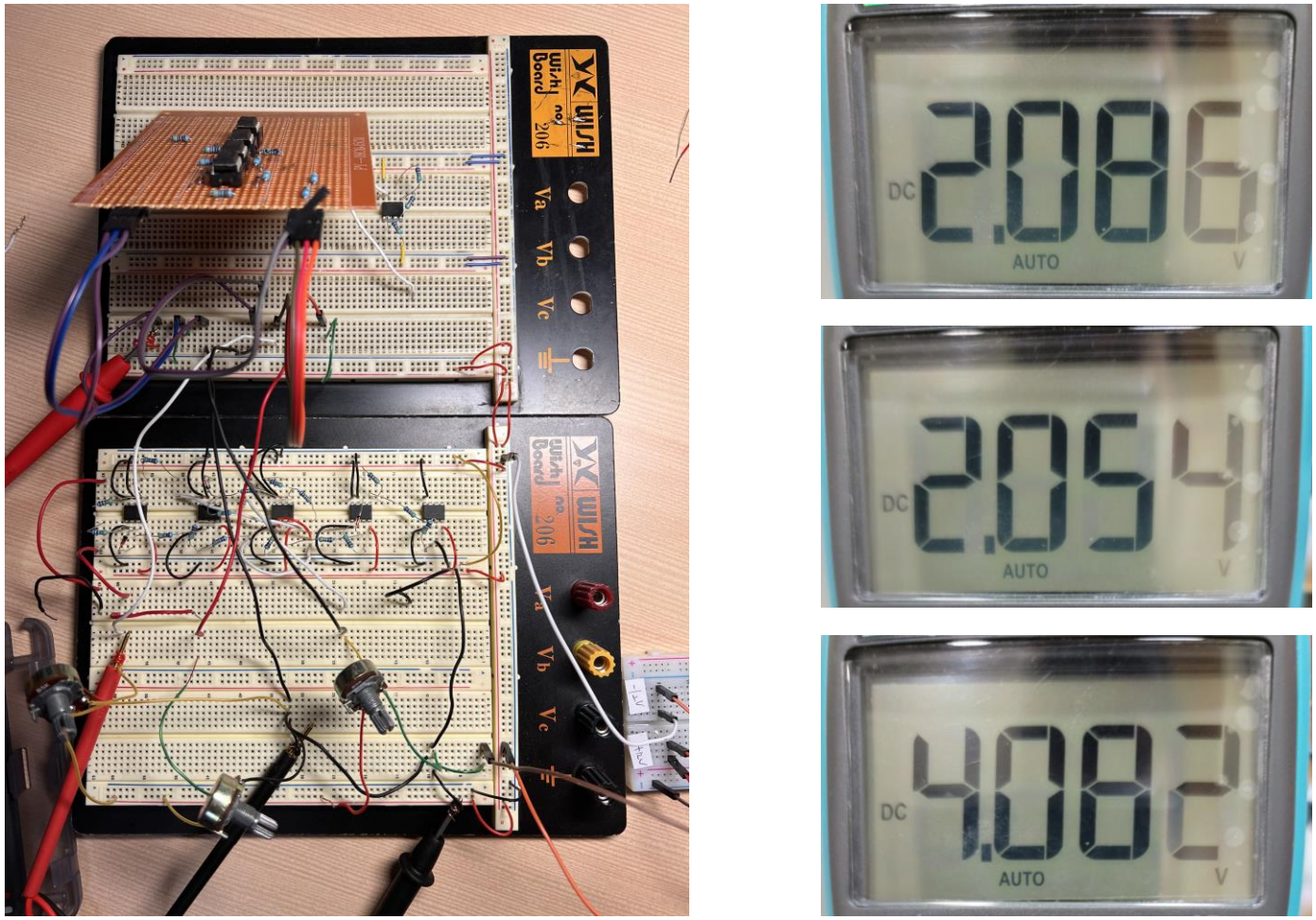


Figure 53. Testing Multiplication Module

Testing Modules (Cont.)

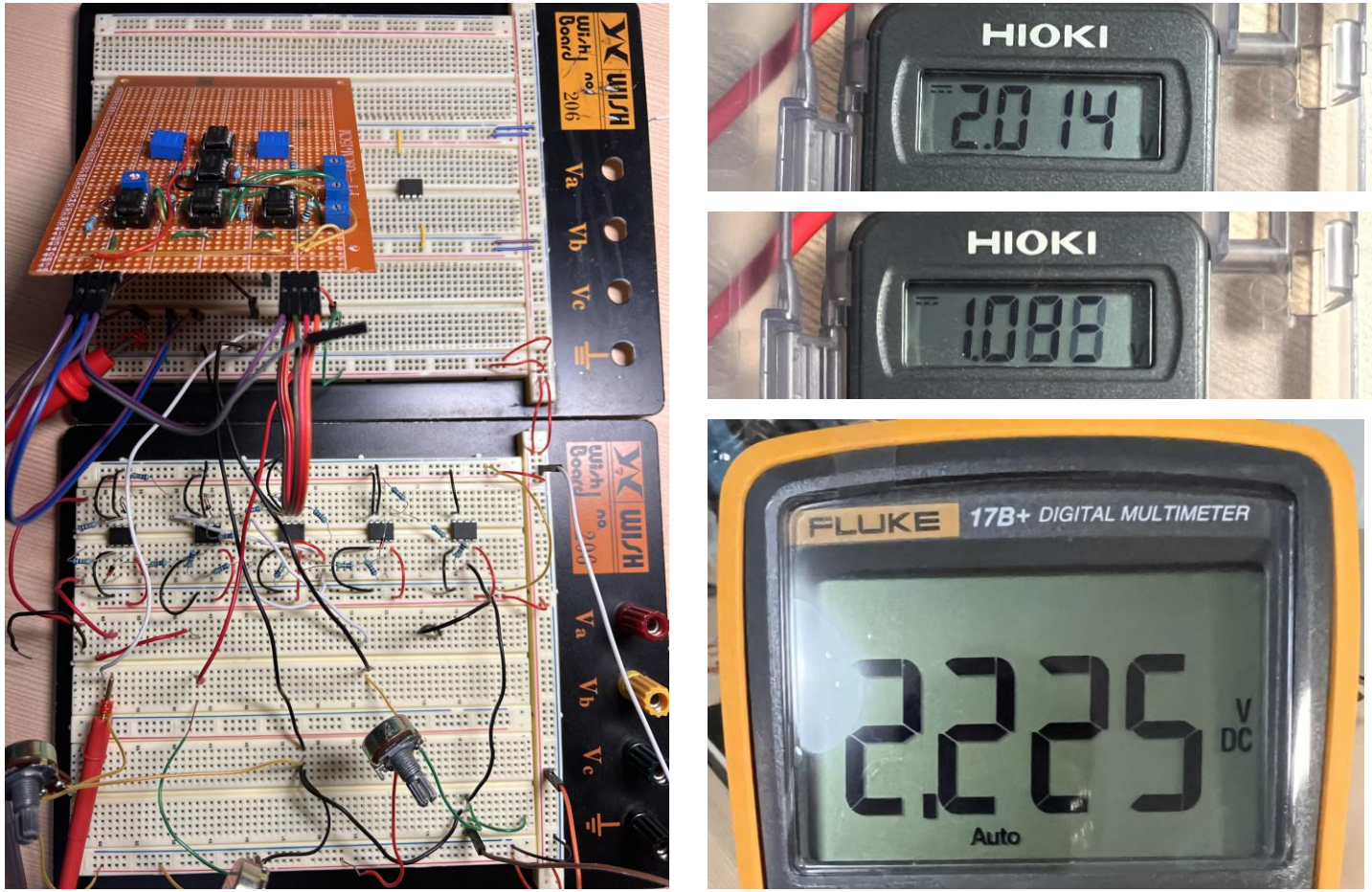


Figure 54. Testing Division Module

Testing Modules (Cont.)

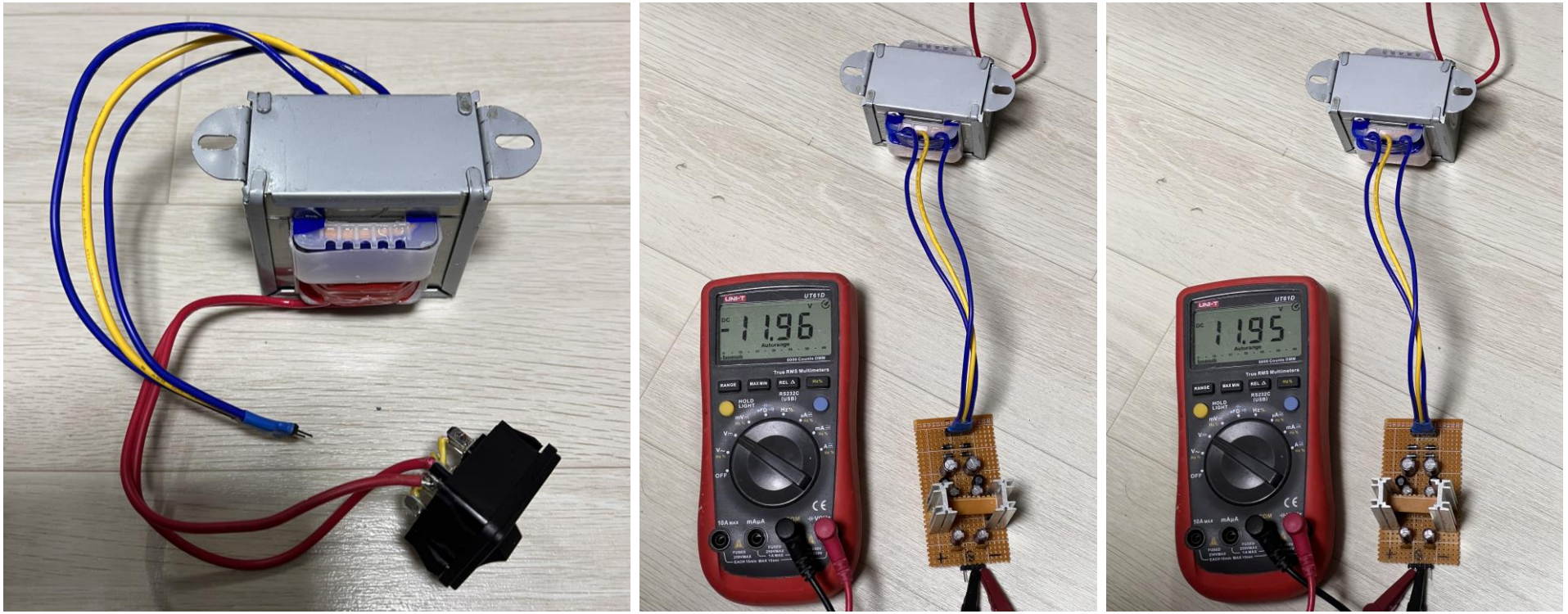


Figure 55. Testing Power Supply Module

Integrating Project

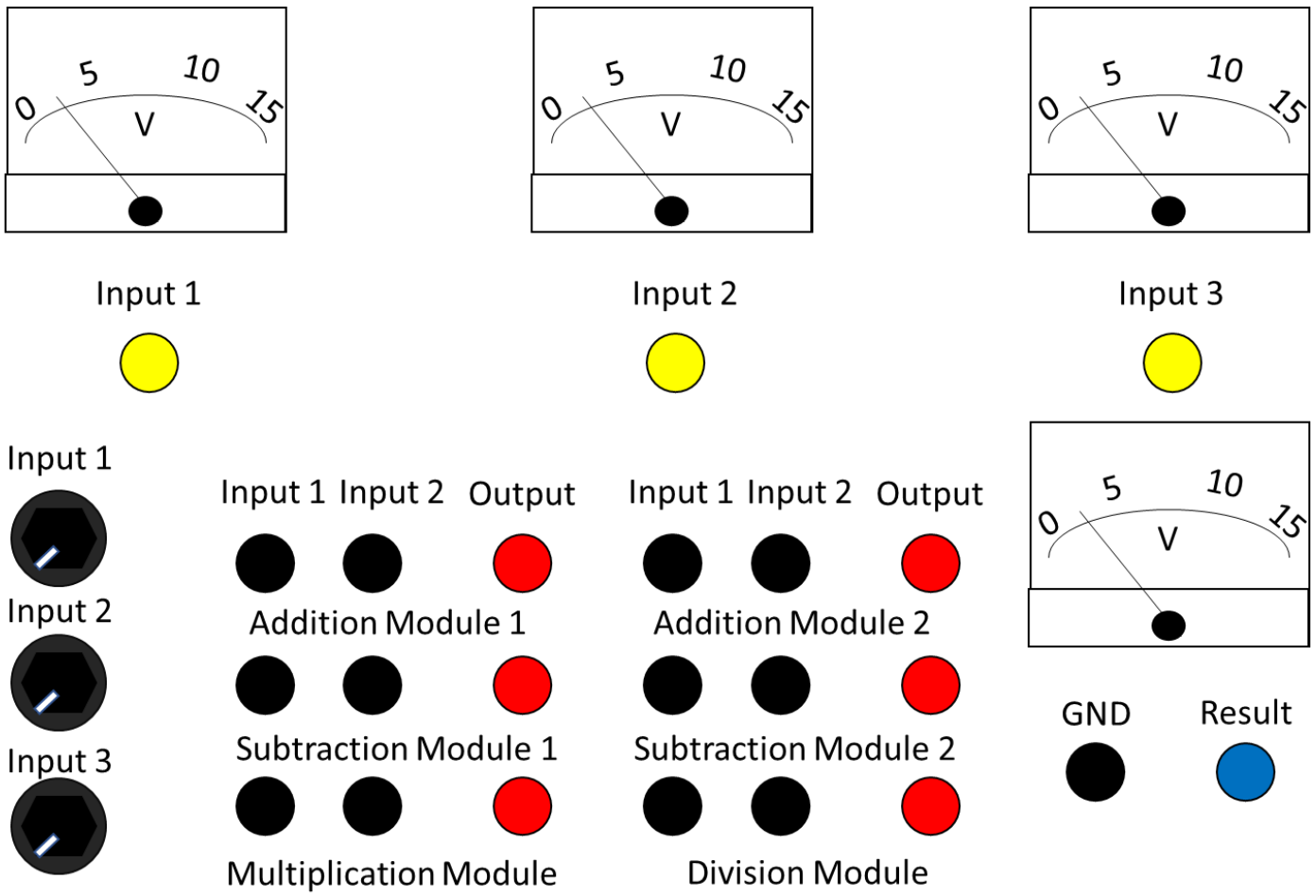


Figure 56. Front Panel Module Input and Outputs of the Calculator, Source: Made with PowerPoint

Integrating Project (Cont.)

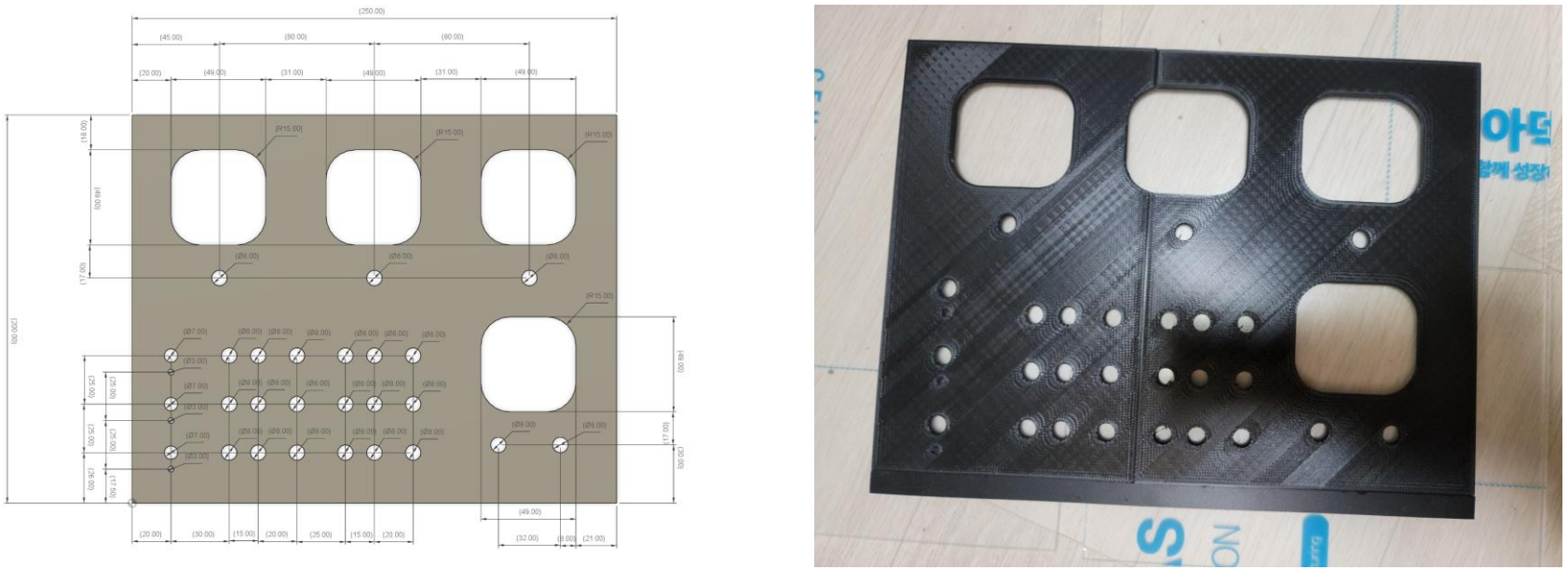


Figure 57. Front Panel designed on Fusion 360 (Left) and Printed Front Panel Using 3D Printer (Right), Source: [12]

- Courtesy of Jiwon Kang's help with the Front Panel.

Integrating Project (Cont.)

Figure 58. Soldering the Panel of the Calculator

Integrating Project (Cont.)

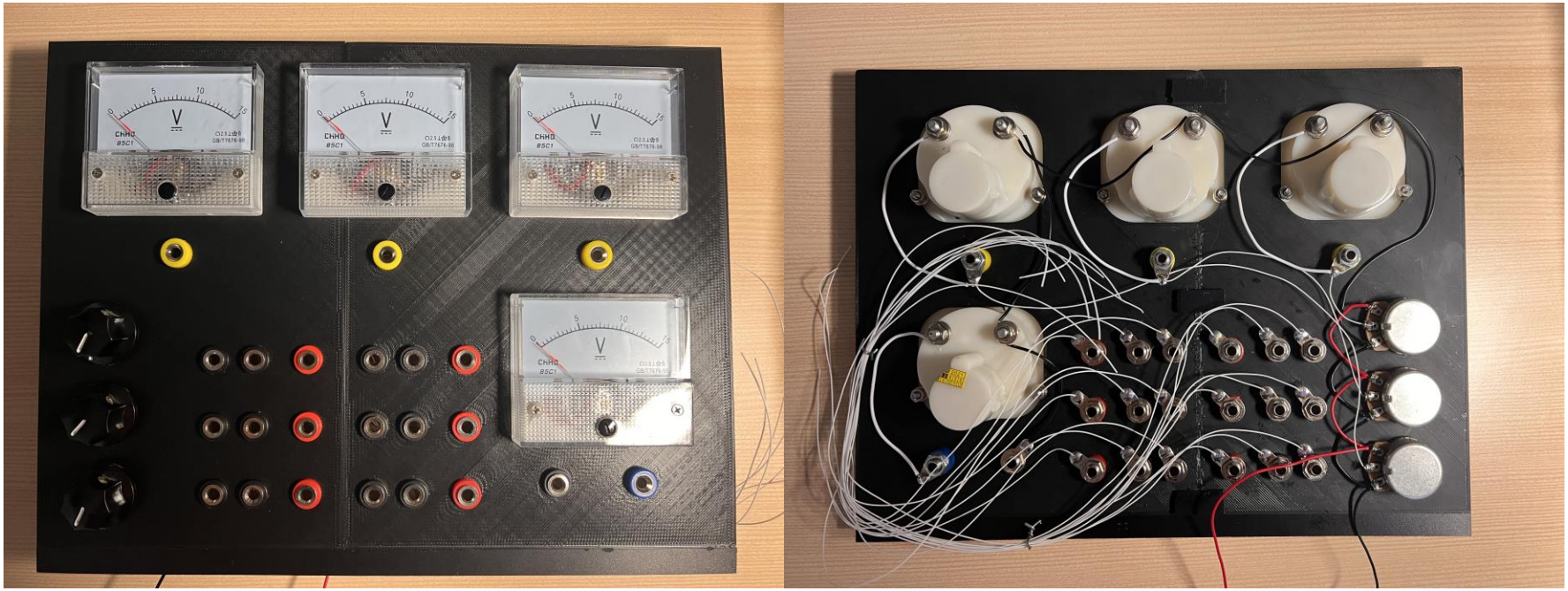


Figure 59. Front Panel (Left) Back Panel (Right) of the Calculator

Integrating Project (Cont.)

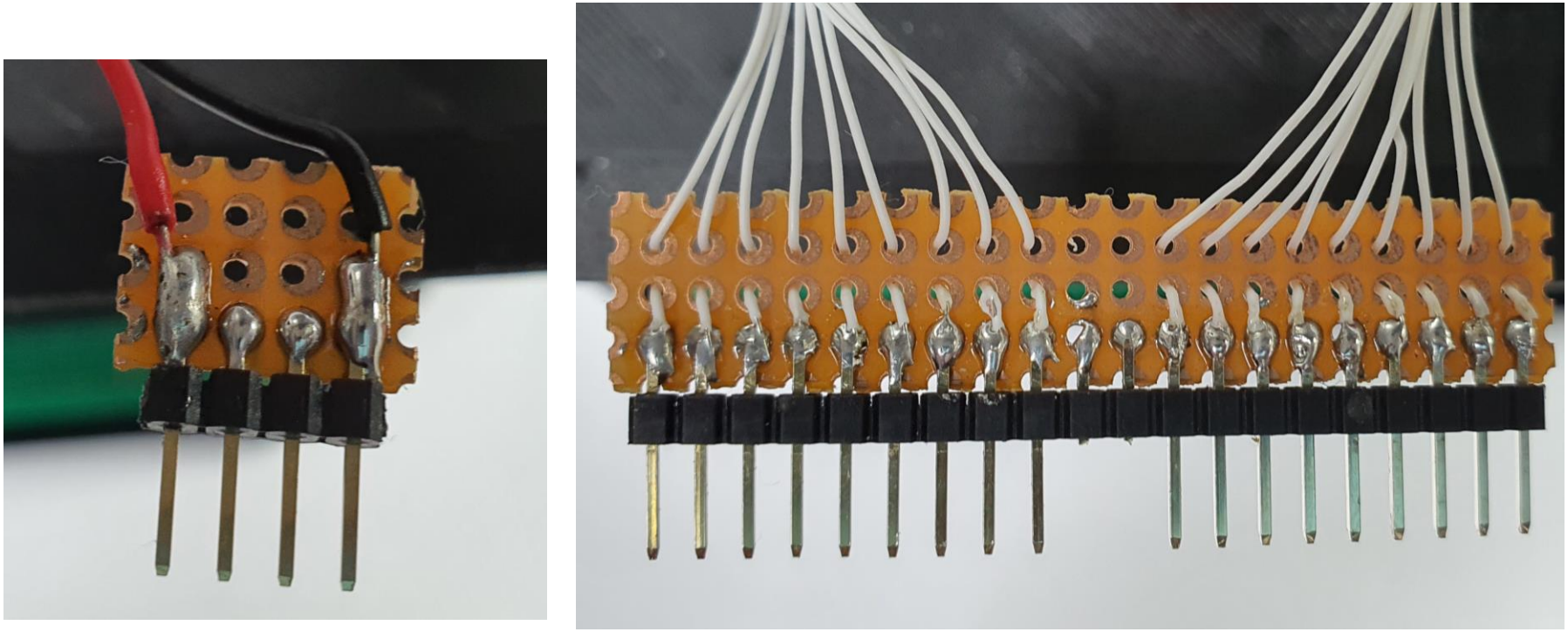


Figure 60. Soldering Power Pins (Left) Soldering I/O Pins (Right) of the Calculator

Integrating Project (Cont.)

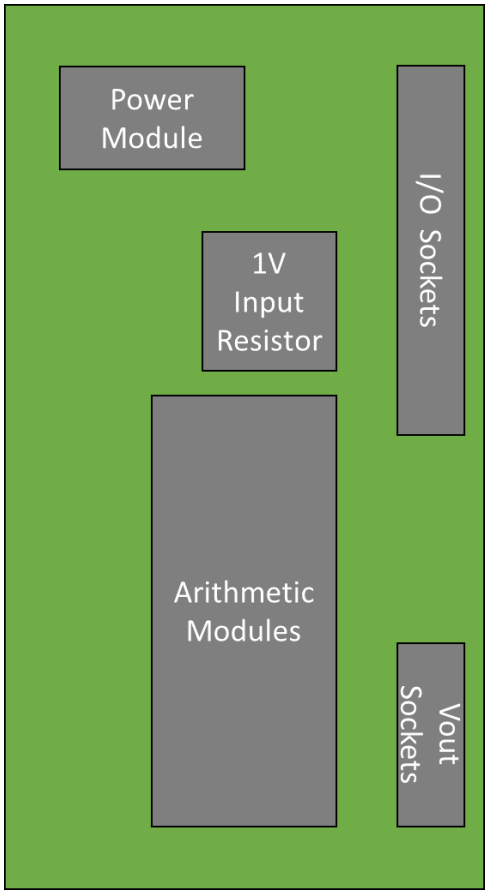


Figure 61. Mainboard Layout, Source: Made with PowerPoint

Integrating Project (Cont.)

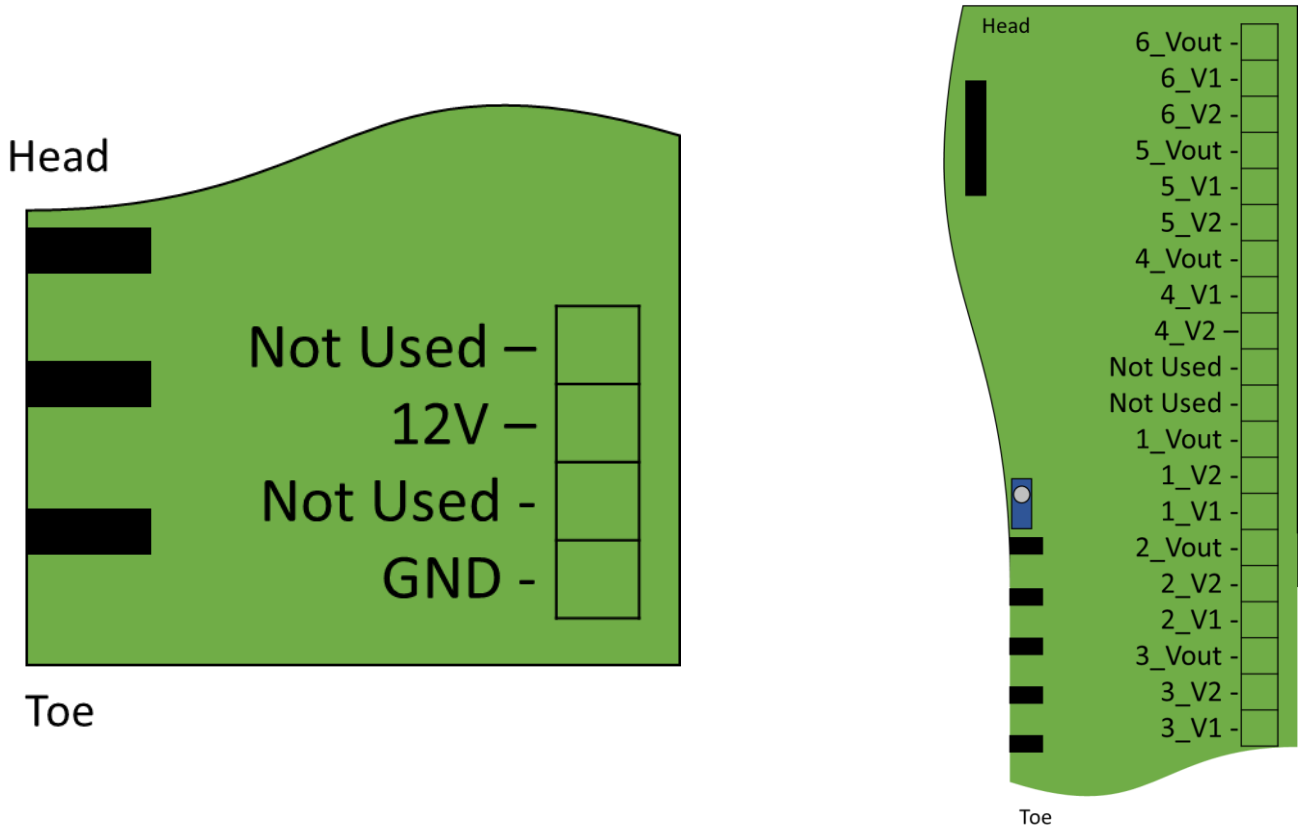
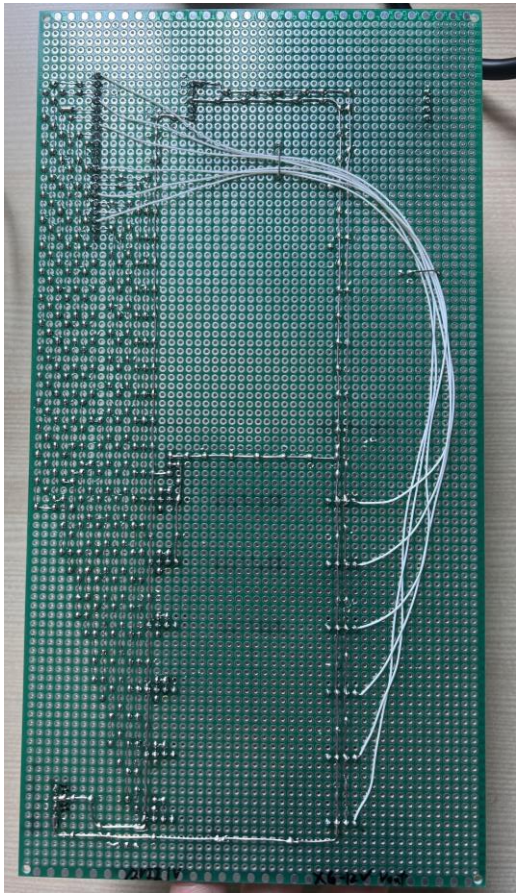


Figure 62. Pin Configuration for the Mainboard, Source: Made with PowerPoint

Integrating Project (Cont.)



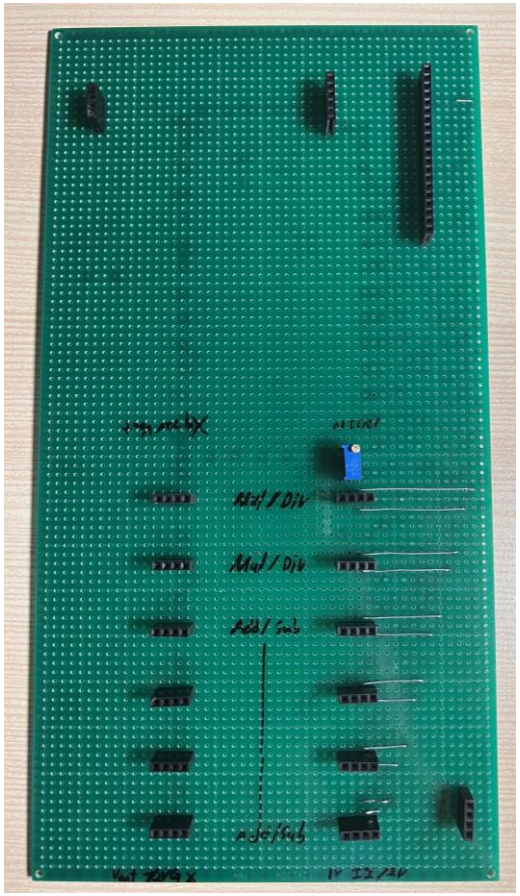


Figure 63. Mainboard Module Arrangements of the Calculator

Integrating Project (Cont.)

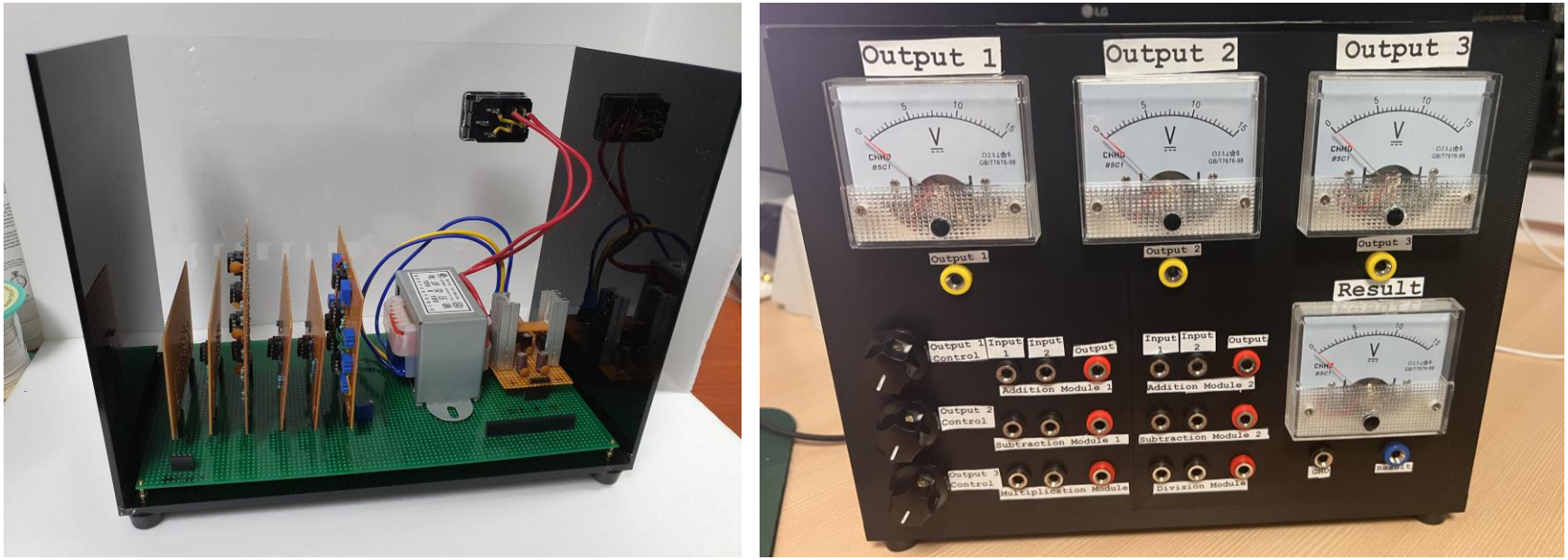


Figure 64. Assembling the Calculator (Left) and the Final Product of the Calculator (Right)

Testing Project

- How did we test our project?

$$Relative\ Error = \frac{|Measured\ Value - True\ Value|}{True\ Value} \times 100\%$$

- When the numerator is not “zero”.

$$Relative\ Error = \frac{|Measured\ Value - True\ Value|}{1 + Measured\ Value} \times 100\%$$

- When the numerator is “zero”.

Testing Project (Cont.)

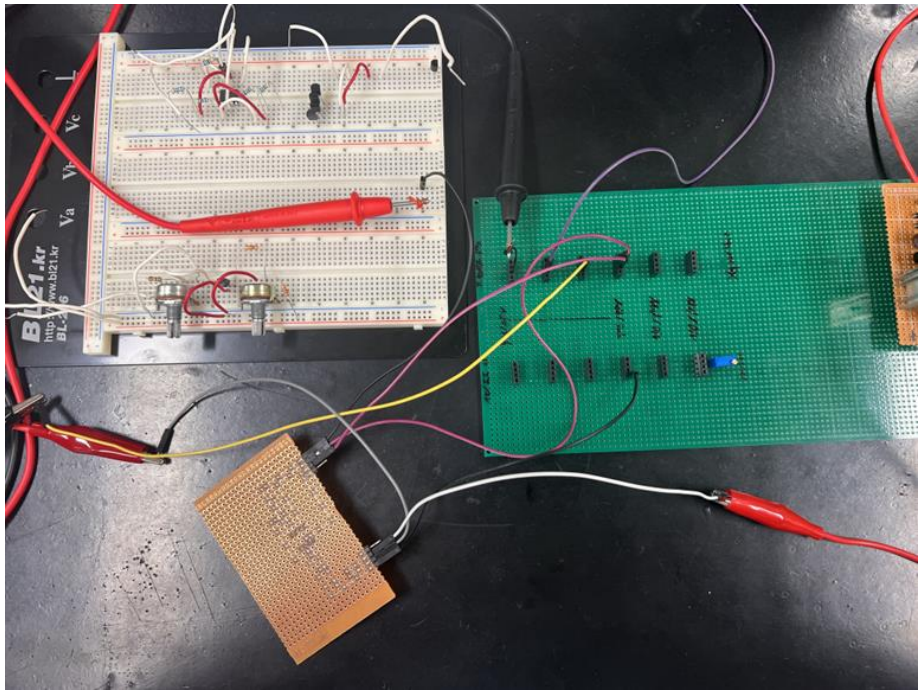


Table 1. Addition error, Source: Made with Excel

Input 1	Input 2	Output	True Value	% Error
1	0	1.021	1	2%
1	1	2.045	2	2%
1	2	3.038	3	1%
1	3	3.993	4	0%
1	4	5.03	5	1%
1	5	6	6	0%
1	6	7.033	7	0%
1	7	7.992	8	0%
1	8	8.974	9	0%
1	9	9.978	10	0%
1	10	10.482	11	5%
1	11	10.482	12	13%
Average Error				2%

Figure 65. Testing the Addition Module (Left) Measured Values and errors in Addition Module (Right)

Testing Project (Cont.)

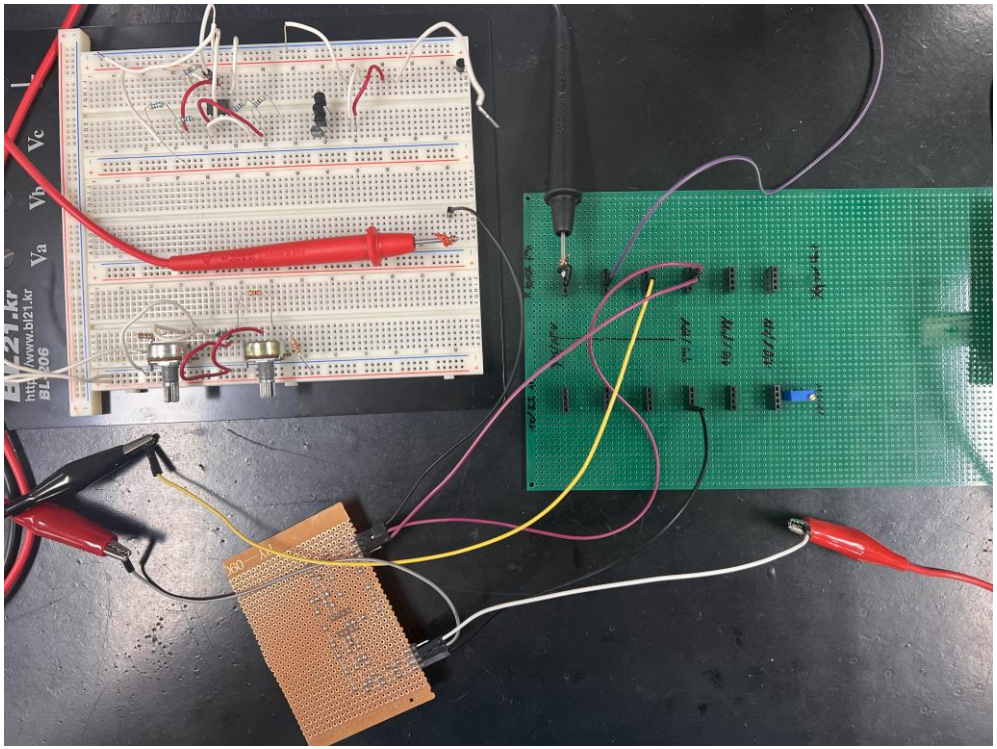


Table 2. Subtraction error, Source: Made with Excel

Input 1	Input 2	Output	True Value	% Error
1	0	1.051	1	5%
1	1	0.053	0	5%
1	2	-0.915	-1	9%
1	3	-1.934	-2	3%
1	4	-2.881	-3	4%
1	5	-3.883	-4	3%
1	6	-4.889	-5	2%
1	7	-5.878	-6	2%
1	8	-6.849	-7	2%
1	9	-7.847	-8	2%
1	10	-8.855	-9	2%
1	11	-9.837	-10	2%
1	12	-10.803	-11	2%
Average Error				3%

Figure 66. Testing the Subtraction Module (Left) Measured Values and errors in Subtraction Module (Right)

Testing Project (Cont.)

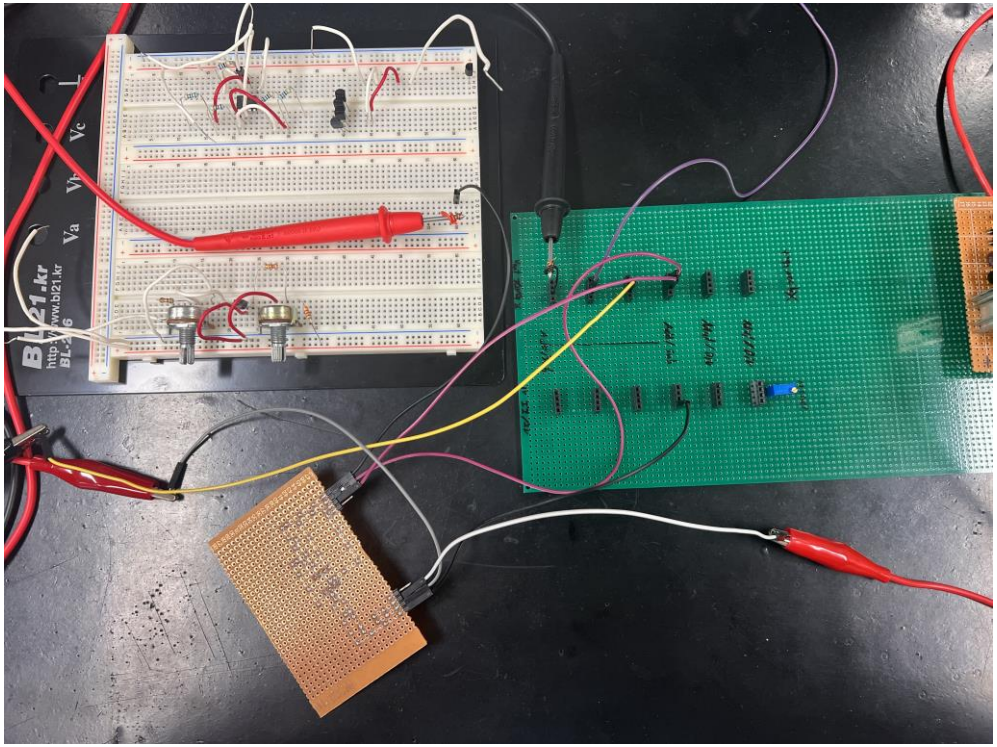


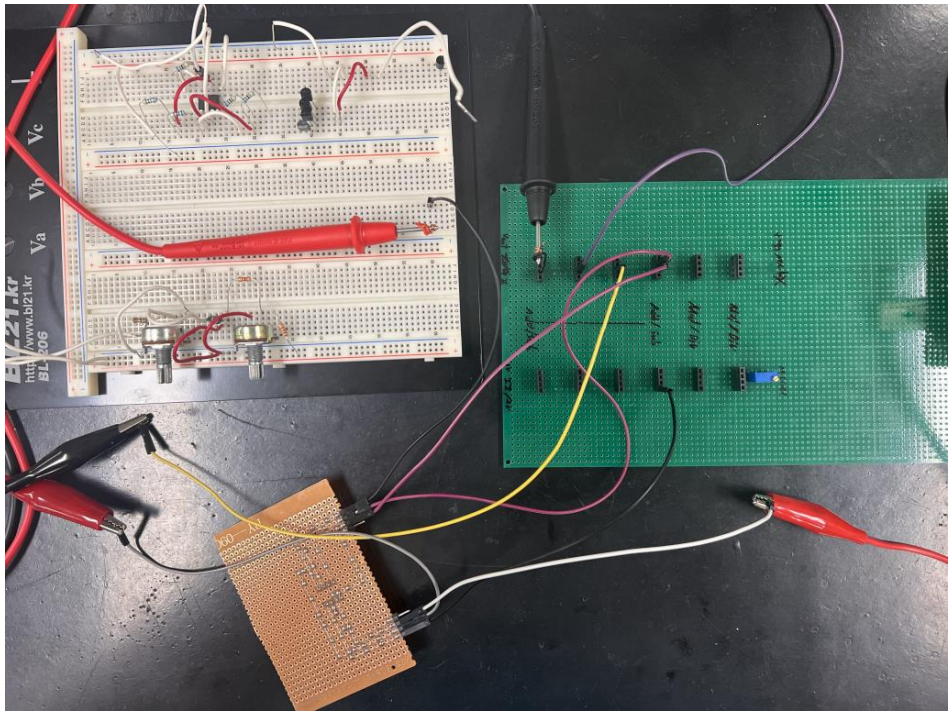
Table 3. Multiplication error, Source: Made with Excel

Input 1	Input 2	Output	True Value	% Error
0	0	2.999	Infinite	X
0	1	0.018	0	2%
0	2	0.015	0	2%
0	3	0.013	0	1%
0	4	0.013	0	1%
0	5	0.011	0	1%
0	6	0.012	0	1%
0	7	0.012	0	1%
0	8	0.012	0	1%
0	9	0.012	0	1%
0	10	0.012	0	1%
0	11	0.012	0	1%
0	12	0.012	0	1%
Average Error				1%

Figure 67. Testing the Multiplication Module (Left) Measured Values and errors in Multiplication Module (Right)

Testing Project (Cont.)

Table 4. Division error, Source: Made with Excel



Input 1	Input 2	Output	True Value	% Error
0	0	2.999	Infinite	X
0	1	0.018	0	2%
0	2	0.015	0	2%
0	3	0.013	0	1%
0	4	0.013	0	1%
0	5	0.011	0	1%
0	6	0.012	0	1%
0	7	0.012	0	1%
0	8	0.012	0	1%
0	9	0.012	0	1%
0	10	0.012	0	1%
0	11	0.012	0	1%
0	12	0.012	0	1%
Average Error				1%

Figure 68. Testing the Division Module (Left) Measured Values and errors in Division Module (Right)

Testing Project (Cont.)

Table 5. Addition Saturation Table, Source: Made with Excel

0	11	10.48	11	5%
0	12	10.48	12	13%
9	2	10.487	11	5%
9	3	10.487	12	13%

Table 6. Subtraction Saturation Table, Source: Made with Excel

12	0	10.483	12	13%
12	1	9.61	11	13%
12	2	8.583	10	14%
12	3	7.599	9	16%
12	4	6.661	8	17%
12	5	5.667	7	19%
12	6	4.691	6	22%
12	7	3.661	5	27%
12	8	2.655	4	34%
12	9	1.708	3	43%
12	10	0.742	2	63%
12	11	-0.291	1	129%
12	12	-1.216	0	122%

Table 7. Multiplication Saturation Table, Source: Made with Excel

1	11	10.47	11	5%
1	12	10.47	12	13%
2	6	10.42	12	13%
6	2	10.44	12	13%
11	1	10.49	11	5%
12	1	10.49	12	13%

Table 8. Division Saturation Table, Source: Made with Excel

12	1	10.54	12.000	12%

- Examples of Saturation Regions in each Modules.

Testing Project (Cont.)

Table 9. Noteworthy Operation in the Division Module, Source: Made with Excel

Input 1	Input 2	Output	True Value	% Error
0	0	2.999	Infinite	X
1	0	10.55	Infinite	X
2	0	10.55	Infinite	X
3	0	10.55	Infinite	X
4	0	10.56	Infinite	X
11	0	10.53	Infinite	X
12	0	10.53	Infinite	X

- Noteworthy Operation, when the numerator is divided by “Zero”.

Testing Project (Cont.)

Table 9. Summary of error rate, Source: Made with Excel

	Addition	Subtraction	Multiplication	Division
Total Average Error for Each module	4%	5%	8%	3%
Average Error Without Saturation Region	1%	2%	7%	3%
Overall Average Error Without Saturation Region	3%			

- Our objective was to make operation errors between 5% ~ 10%.

Testing Project (Cont.)

- How accurate is it, when the values are calculated more than once?

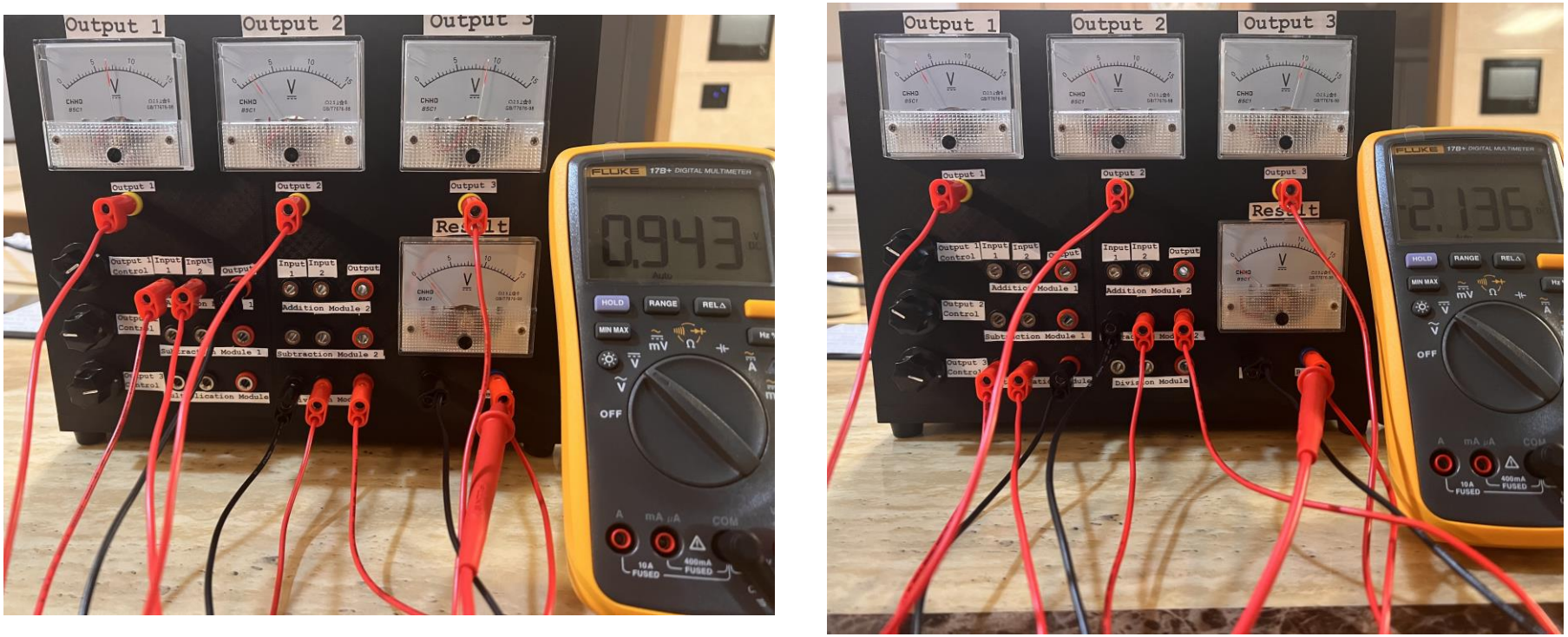


Figure 69. Best case: (7 + 2) / 9 = 1 (0.943, error 6%) (Left)
Worst case: (3 * 3) - 10 = -1 (-2.136, error 114%) (Right)

Final Product (Cont.)

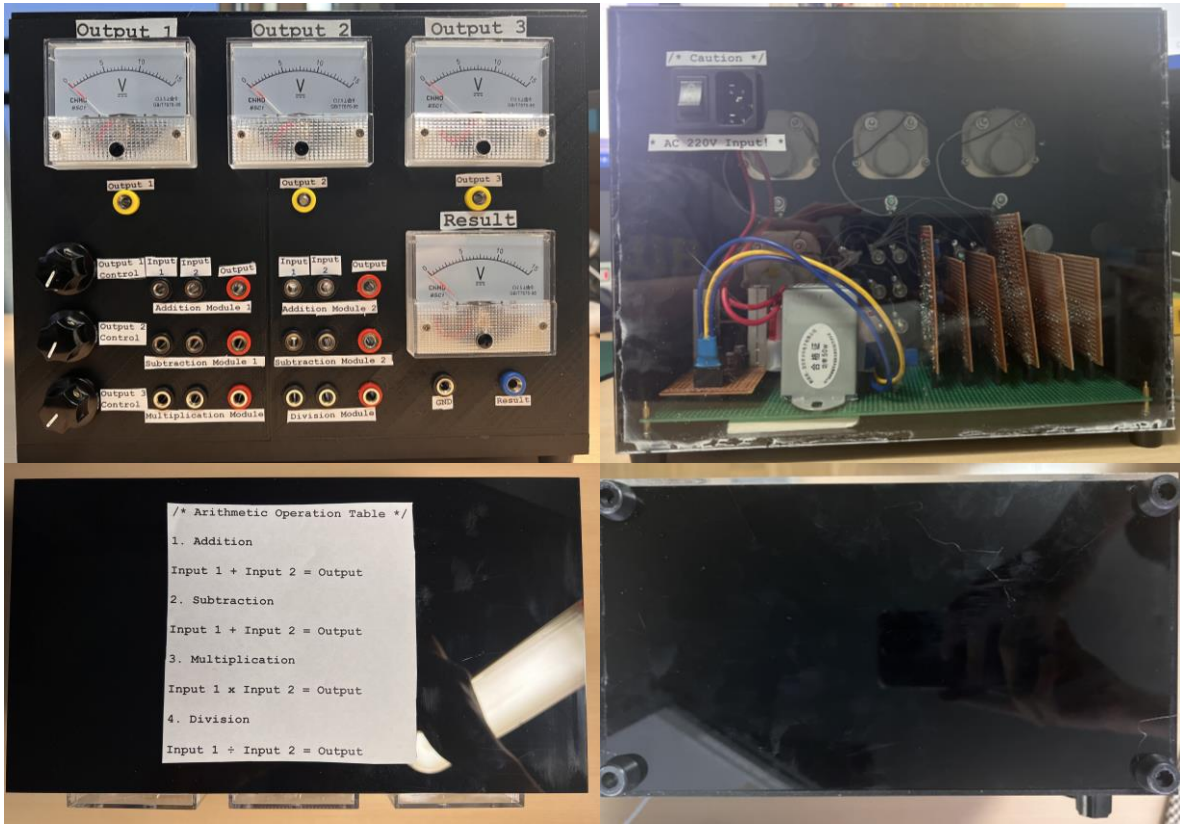


Figure 70.Front, Back, Top, Bottom (From Left to Right and Top to Bottom)

Final Product (Cont.)

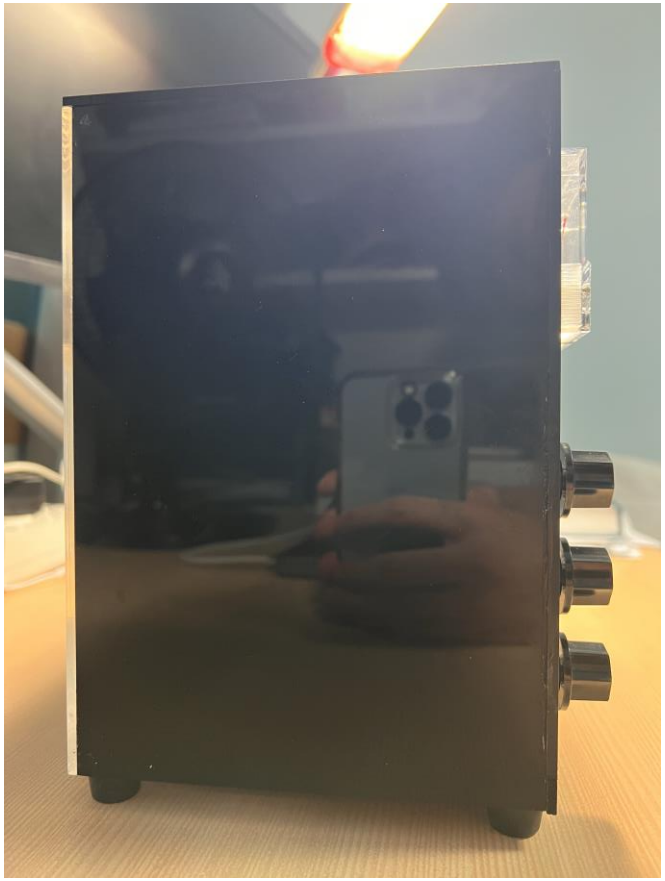
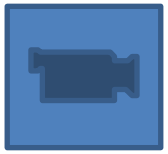


Figure 71.Right Side of the Calculator (Left) and Right Side of the Calculator (Right)

Demo

- Short clip of our product demonstration.



Demo (Cont.)

- Demonstration

CHAPTER 3 : AFTERMATH

Debugging & Additional Feature

- **Task 1. Division Circuit**
  - The computer simulation did not work at all.
  - Output false values.

- **Task 2. Multiplication Circuit**
  - Dropdown needs to lower for less error
  - Ripple voltages Inputs

- **Task 3. Power Module**
  - Power Module would get very hot and would sometimes explode for no apparent reason.

- **Additional Feature**
  - Adding Lights for checking power.

Debugging & Additional Feature – Task 1 (Cont.)

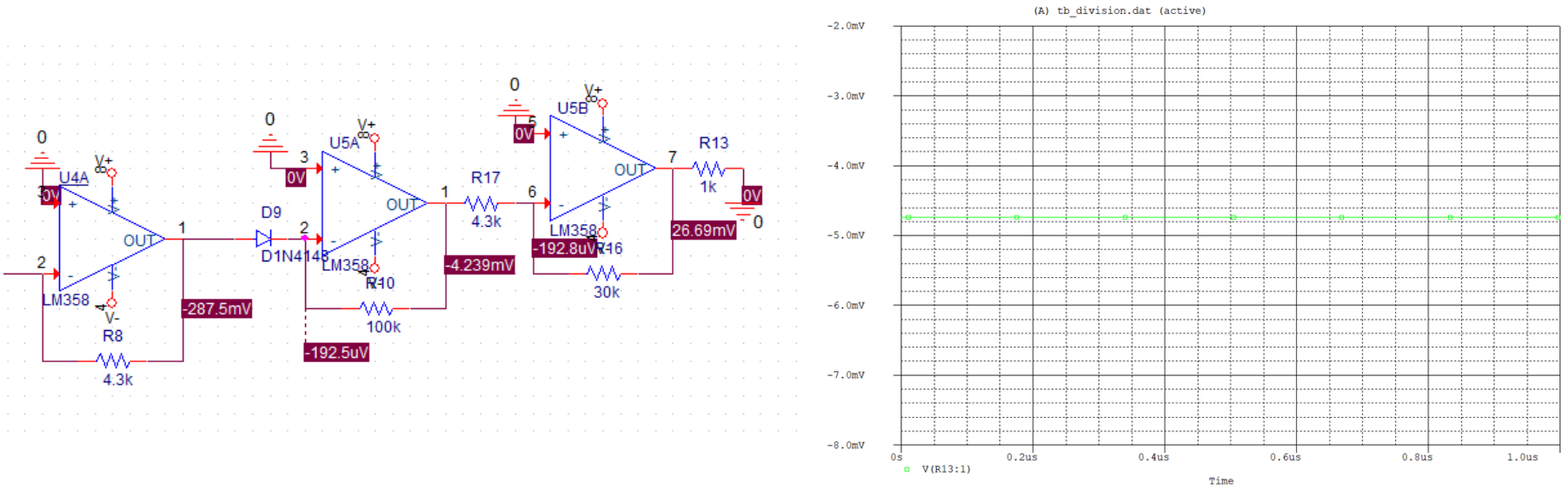
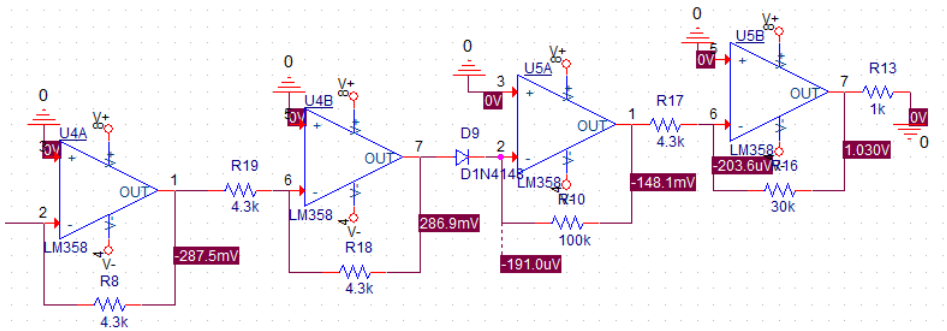


Figure 72. Unstable Circuit before debugged (Left) and Wrong output for 12 / 12 = 1 (Right), Source: Adapted from [3]

Debugging & Additional Feature – Task 1 (Cont.)



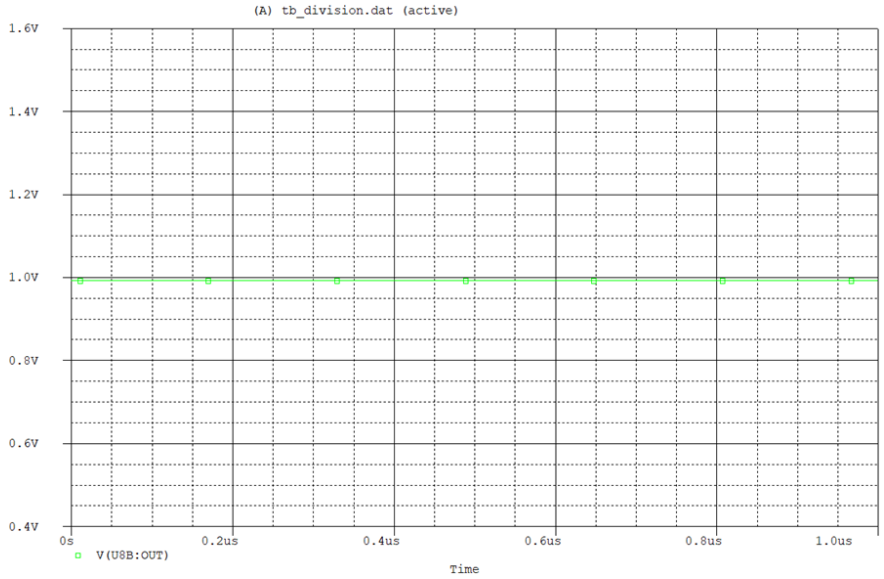


Figure 73. Debugged Circuit Added, an inverting amplifier (Left) Correct output for 12 / 12 = 1 And (Right), Adapted from [3]

Debugging & Additional Feature – Task 1 (Cont.)

Trace Color	Trace Name	Y1
	X Values	0.000
CURSOR 1,2	V(U4B:OUT,U6B:-)	-288.270m

Trace Color	Trace Name	Y1
	X Values	0.000
CURSOR 1,2	V(D5:1,U6B:-)	288.050m

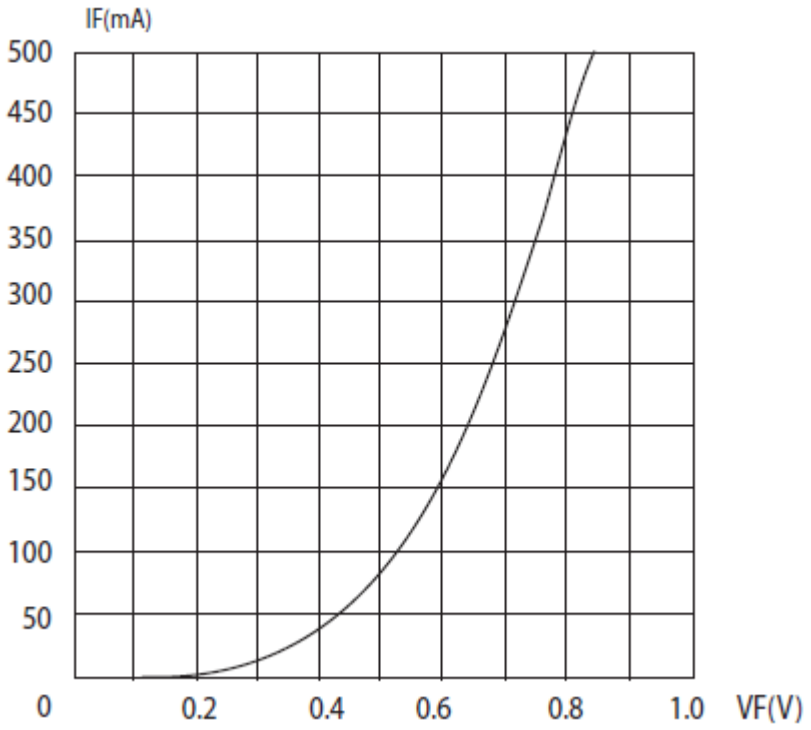


Figure 74. Debugged Before - Top and After - Bottom (Left) I-V Characteristic for 1n60 Diode (Right), Source: Adapted from [3]

Debugging & Additional Feature – Task 1 (Cont.)

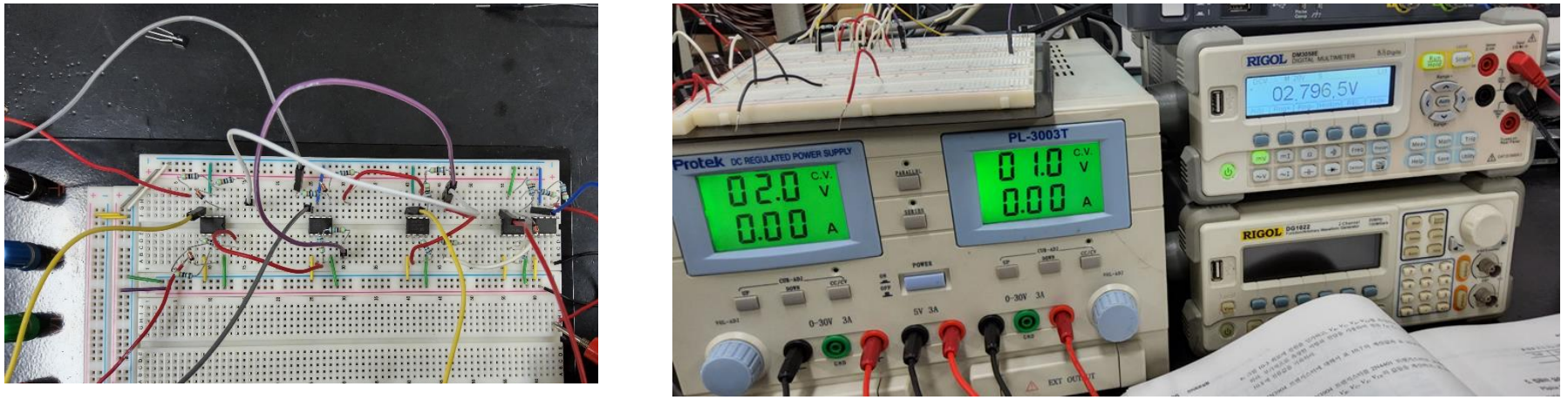


Figure 75. Division Circuit (Left) Division Circuit Result (Right)

Debugging & Additional Feature – Task 1 (Cont.)

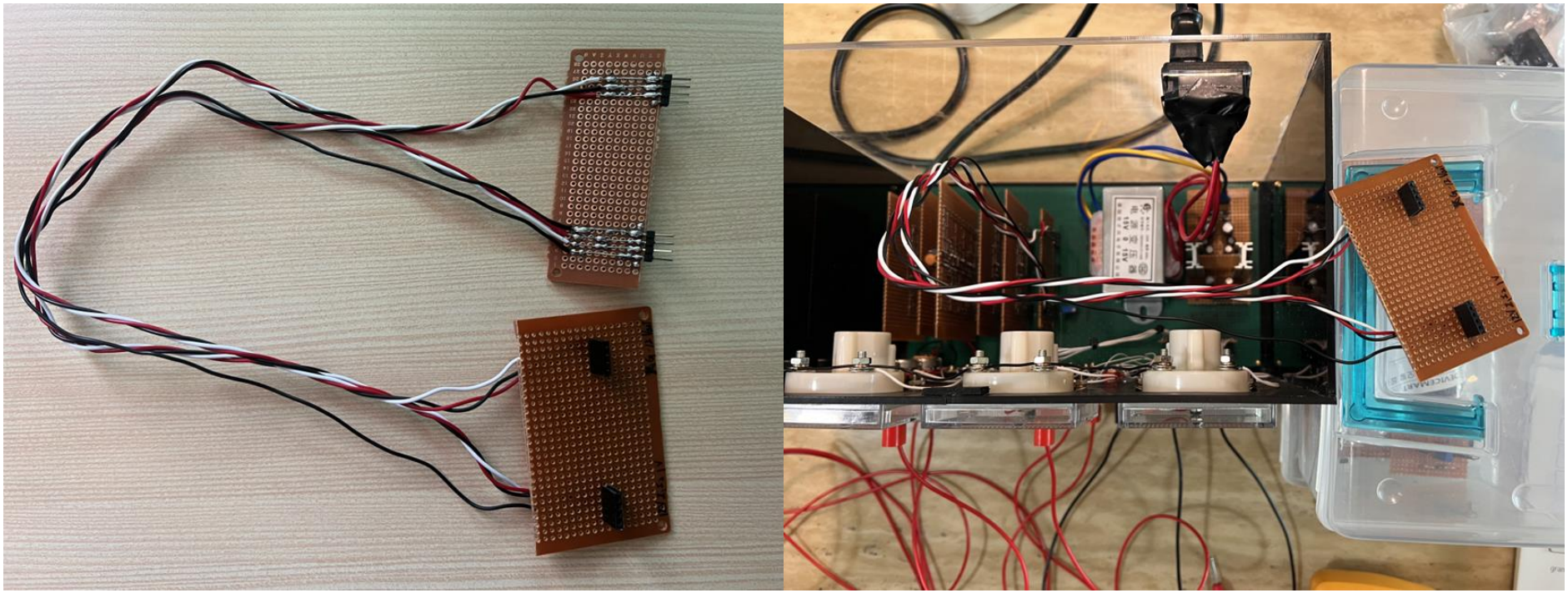


Figure 76. Made a debugging module to debug the division module for better accuracy

Debugging & Additional Feature – Task 1 (Cont.)

- The aspect of the measured voltage values are different to the computer simulation.

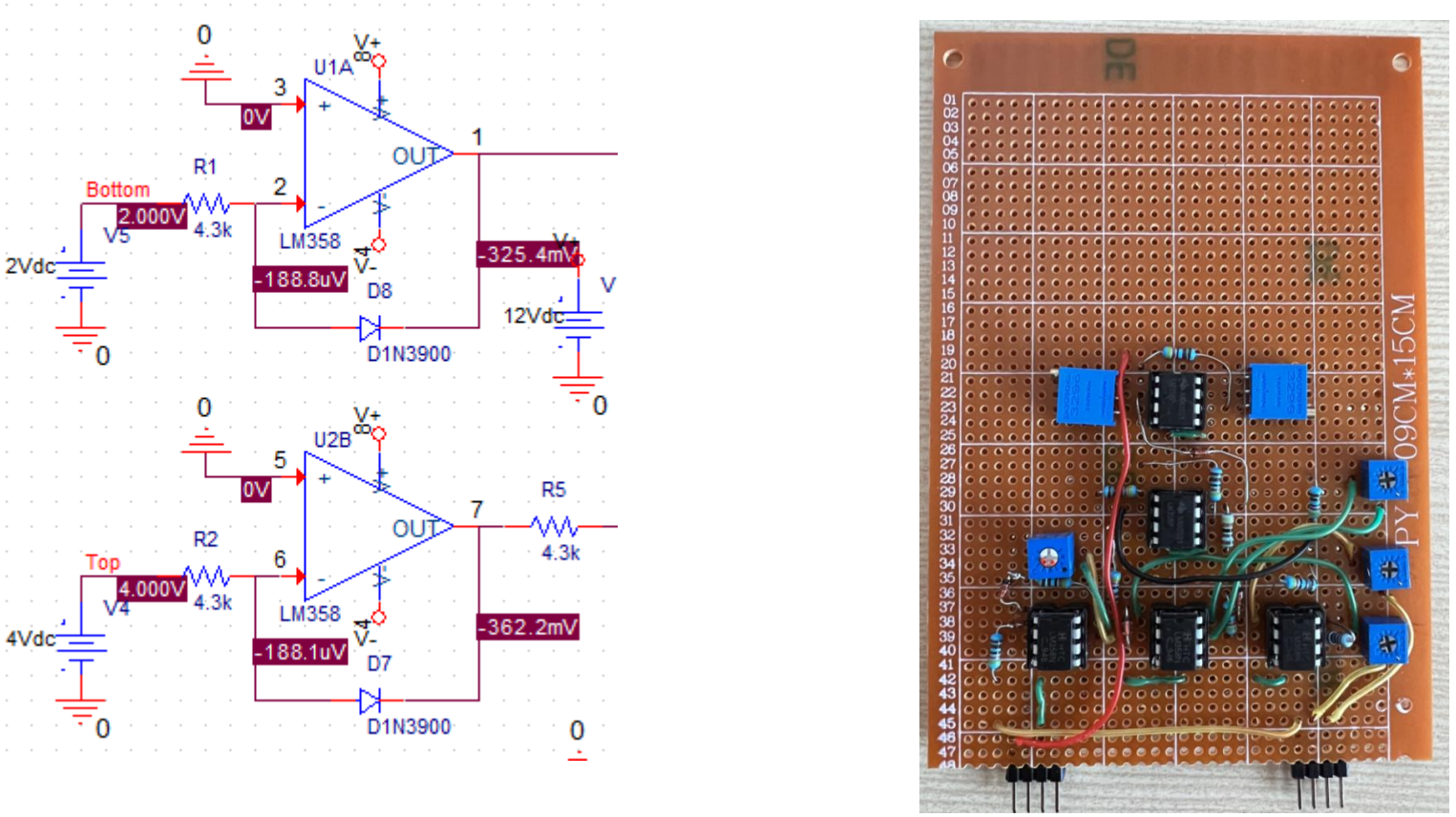
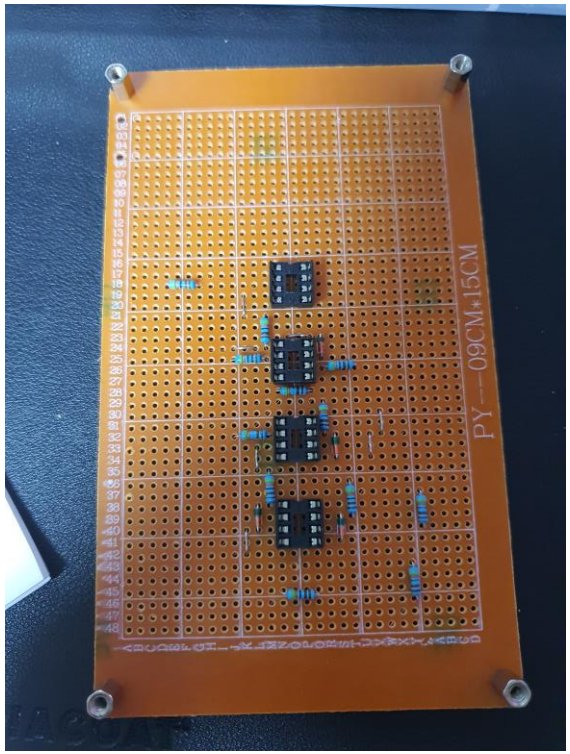


Figure 77. Division Circuit Schematic (Left) and Division Circuit (Right), Source: Adapted from [3]

- Tuned the circuit using potentiometers.

Debugging & Additional Feature – Task 2

- Si, Ge diodes were unstable and replaced them with Schottky diodes



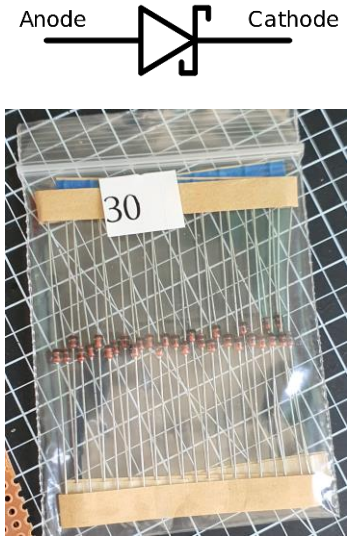
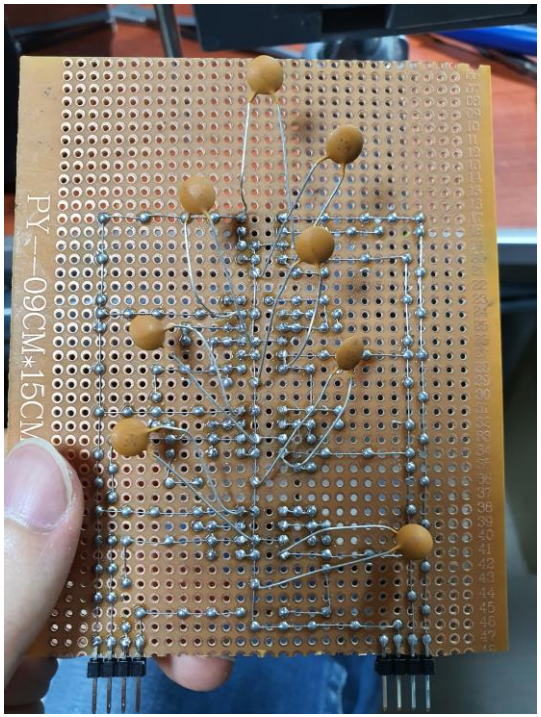


Figure 78. Multiplication Module made with Ge diode(left),
Replacement of Ge Diodes with Schottky diode (right)

Debugging & Additional Feature – Task 2 (Cont.)

- Added decoupling capacitors to stable the ripples made in the input voltages



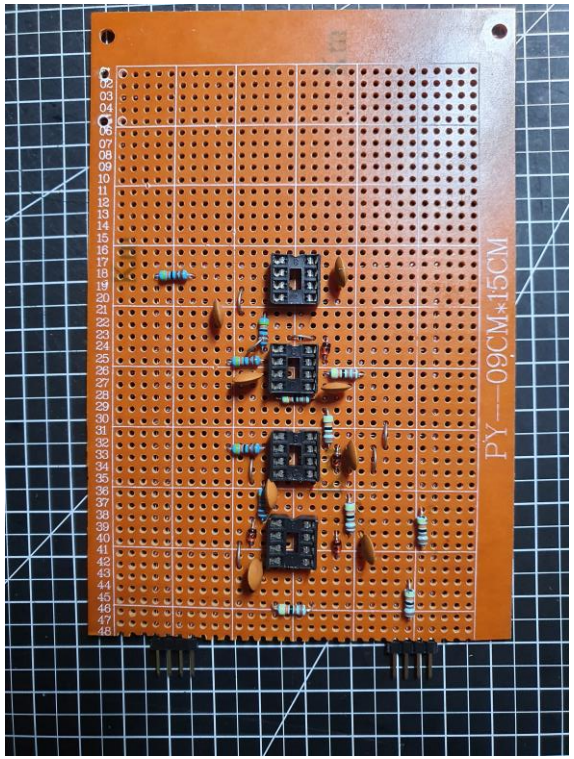
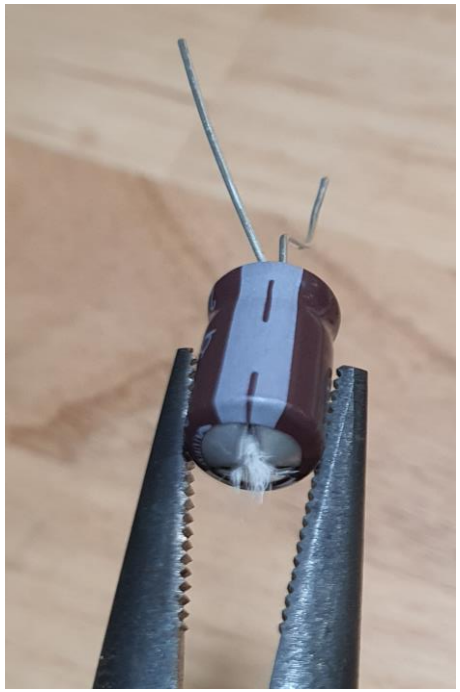
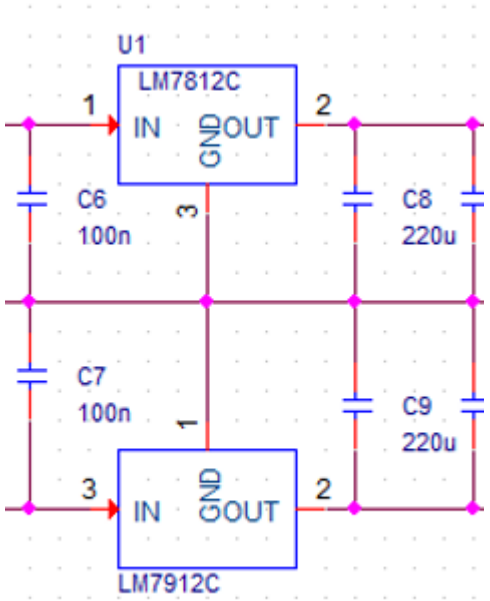


Figure 79. Connecting decoupling Capacitors to +12V/-12V inputs of the module

Debugging & Additional Feature - Task 3 (Cont.)

- All circuit elements must be double checked before turning the power on.





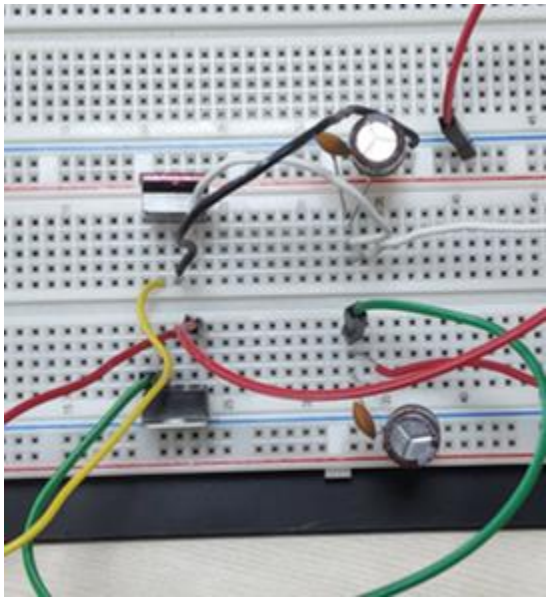


Figure 80.Exploded Capacitor (Left), Circuit Schematic (Middle) and Breadboard (Right), Source: Adapted from [3]

- Because LM7912C has a different voltage polarity to the LM7812C, the capacitor that is connected must be connected opposite of LM7812C.

Debugging & Additional Feature - Task 3 (Cont.)

- All circuit elements must be double checked before turning the power on.

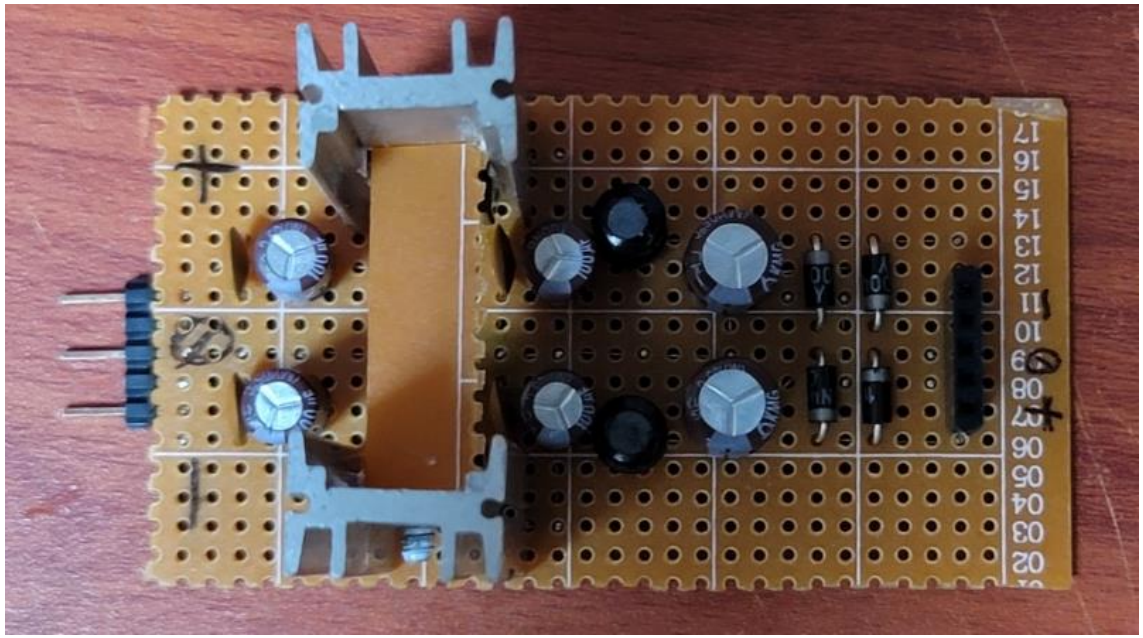


Figure 81.Power Module

- Added heat sinks on both 7812 and 7912 where heat was dissipated the most.
- Added bridge diodes just to make load, to dissipate somewhat voltage on the 7812 and 7912.

Debugging & Additional Feature (Cont.)

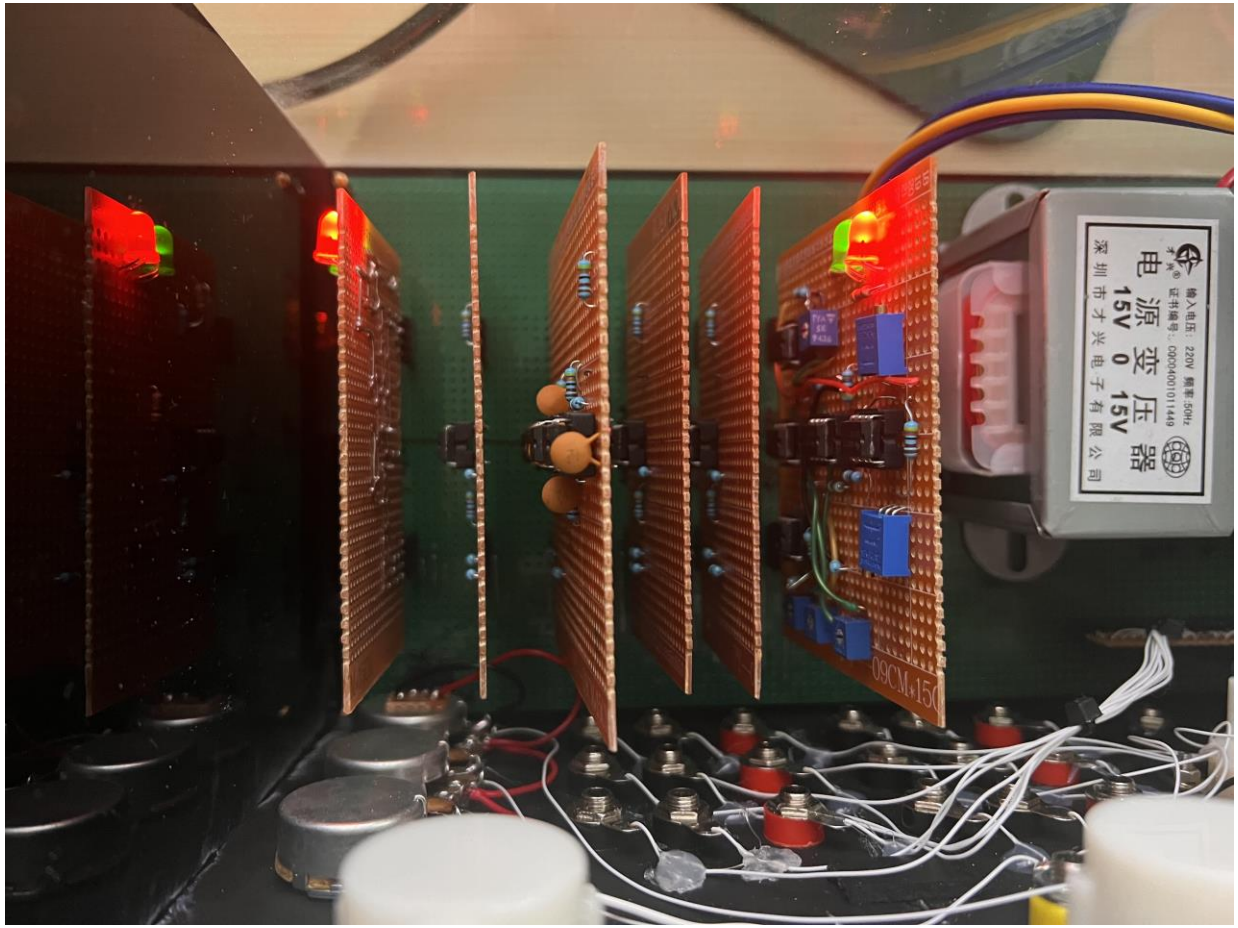


Figure 82.LED added on each end of the modules

- Added LED lights to check if each module is powered correctly.
  - Green LED for +12V
  - Red LED for -12V

Role Division

Table 10. Role Division, Source: Made with Excel

Name	Role
고종완	1. Division Circuit Design 2. PSpice Simulation 3. Module Integration 4. Power Supply Implementation
강승엽	1. Multiplication Circuit Design 2. PSpice Simulation 3. Module Integration 4. Power Supply Implementation
구완모	1. Addition / Subtraction Circuit Design 2. PSpice Simulation 3. Module Integration 4. Power Supply Implementation

Project Timeline

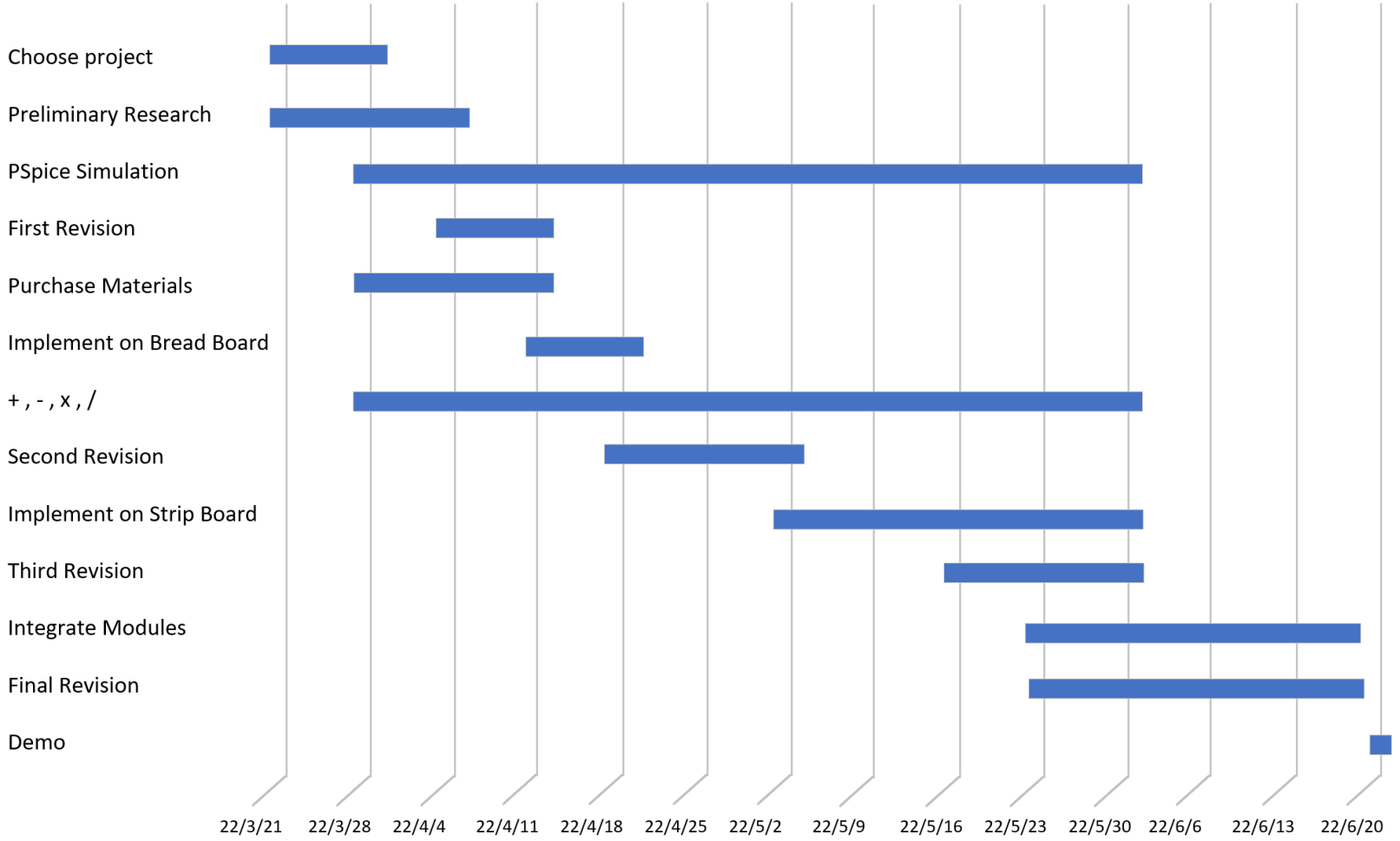


Figure 83.project Timeline, Source: Made from Visio

Project Design Objective

- **Arithmetic Operation**
  - Addition √
  - Subtraction √
  - Multiplication √
  - Division √
  - Overall Output Result Error < 5% √

- **Function**
  - Link output result back to input and calculate given inputs √
  - Measure the result using an Analog Voltmeter √
  - 12V input operation (Even with saturation regions, overall result was a success) √

- **Power Module**
  - Stable Power Supply for Machine √
  - Stable Output Voltage for Arithmetic Operations √

Limitations and Further Improvements

- **Limits**
  - The saturation current is sensitive to temperature. Therefore, if the diodes are not manufactured closely as possible in the silicon wafer, the output of this system will have higher errors than that of an equivalent IC chip.
  - With the Op Amps wired to +12V and -12V, we can not compute beyond this limit.
  - Due to the saturation region in the circuits, it has a limited computing operations than expected.
- **Further Improvements**
  - We can improve this system by manufacturing this system on a single IC chip, instead of making this device using separate parts.
  - We could get more precise results by stabilizing the input voltages, in other words improving a more stable power could reduce the errors.
  - Tune or coordinate the circuits according to the simulation by replacing resistors or diodes. Circuit must be tuned until we gain the desired values.

Components and Budget

Table 12. Shipping Fee, Source: Made with Excel

No.	Shipping Fee	Fee
1	Device Mart (04/06)	₩ 2,700
2	Device Mart (05/05)	₩ 2,700
3	IC114 (05/05)	₩ 2,700
4	IC114 (05/21)	₩ 2,700
5	원테크 (05/11)	₩ 3,000
6	Si Tai&SH IC accessories Store	₩ 1,249
7	Chip-IC Store	₩ 3,211
8	AGUHAJSU Chinese chip Store	₩ 1,249
9	Xin Chuang Instrument & Meter Store	₩ 10,167
10	Yunbcc Store (05/04)	₩ 6,832
11	Device Mart (05/09)	₩ 2,700
12	IC114 (05/18)	₩ 2,700
13	Device Mart (05/22)	₩ 2,700
14	입소문(05/23)	₩ 3,000
15	Device Mart (05/27)	₩ 2,700
Total Shipping Fee		₩ 50,308

Table 13. Tax Fee, Source: Made with Excel

No.	Tax Fee	Fee
1	Device Mart (04/06)	₩ 1,145
2	Device Mart (05/05)	₩ 950
3	IC114 (05/05)	₩ 2,408
4	IC114 (05/21)	₩ 2,580
5	원테크 (05/11)	₩ 289
6	Yunbcc Store (05/04)	₩ 952
7	Device Mart (05/09)	₩ 140
8	IC114 (05/18)	₩ 180
9	Device Mart (05/22)	₩ 690
10	Device Mart (05/27)	₩ 170
Total Tax Fee		₩ 9,504

Components and Budget (Cont.)

Table 13. Total Fee, Source: Made with Excel

No.	Description	Pcs. / Counts	₩ Cost
1	1/4W 1% Axial Resistor 432F (1KΩ)	50	₩ 1,250
2	1/4W 1% Axial Resistor 432F (4.3KΩ)	50	₩ 1,250
3	1/4W 1% Axial Resistor 432F (10KΩ)	50	₩ 1,250
4	1/4W 1% Axial Resistor 432F (1MΩ)	50	₩ 1,250
5	1N4148	30	₩ 450
6	LM358N	20	₩ 6,000
7	POWER AC CODE (220V용/1.5M) [P3211]	1	₩ 1,500
8	범용 페놀 만능 PCB 기판 90X150-단면 [PCB-0915P]	10	₩ 4,400
9	SS-120BEL	2	₩ 3,600
10	1N4004-0.7T 1N4004	40	₩ 640
11	A2-40PA-DSA-11.5MM	2	₩ 240
12	CG50VF104Z06BS 0.1UF50VDC	60	₩ 1,800
13	FH01-04SSJ1-4PDSA	20	₩ 1,000
14	IR10MM-101(100uH)	20	₩ 5,000
15	JB-600BK JB600BK	14	₩ 3,500
16	JB-600R JB600R	6	₩ 1,500
17	KA431AZ431	10	₩ 1,400
18	KMG107M1E100UF25V	20	₩ 900
19	KMG227M1E220UF25V	20	₩ 1,200
20	MC7912CTG7912(RoHS)	10	₩ 3,900

Components and Budget (Cont.)

No.	Description	Pcs. / Counts	₩ Cost
21	NJM7812A7812A	10	₩ 2,000
22	2401-20SL-B5KVR24MM5K	4	₩ 2,000
23	3296W-502-LF(58W-502) SVR5K-3296	20	₩ 5,000
24	HSE-2513SPCB-2513S	2	₩ 16,000
25	HS-RN-B01-6.0B01	4	₩ 2,800
26	바나나 플러그-바나나 플러그 케이블 1M (black)	2	₩ 4,000
27	바나나 플러그-바나나 플러그 케이블 1M (red)	8	₩ 16,000
28	10PCS IC Sockets DIP8	5	₩ 3,935
29	10PCS LM358P DIP8	5	₩ 3,750
30	100pcs/lot 1N4148	1	₩ 600
31	100pcs Metal film resistor series 1/4W 1% 1M	2	₩ 1,100
32	100pcs Metal film resistor series 1/4W 1% 10k	2	₩ 1,100
33	100pcs Metal film resistor series 1/4W 1% 1k	2	₩ 1,100
34	100pcs Metal film resistor series 1/4W 1% 4.3k	2	₩ 1,100
35	YX-360TRd Analog Multimeter AC DC Volt Ohm Current Testing Electrical Multitester	1	₩ 18,255
36	85C1 DC Analog Panel Volt Voltage Meter Voltmeter Gauge Mechanical Voltage Meter 5V	6	₩ 7,758
37	50W Power Transformer Input AC 220V 50HZ Output AC 15V Dual	1	₩ 35,184
38	핀헤더 Single 1x40Pin Straight(2.54mm)	10	₩ 1,400
39	Schottky Diode 40V,30mA,VF0.37V	30	₩ 1,800
40	바나나잭(JB-601) 옵션: 파랑	2	₩ 1,200

Components and Budget (Cont.)

No.	Description	Pcs. / Counts	₩ Cost
41	바나나잭(JB-601) 옵션: 노랑	4	₩ 2,400
42	스프링와샤 M2	10	₩ 200
43	스텐 둥근머리 십자볼트 M2x12	10	₩ 400
44	PCB 서포트 황동 2.5 파이 M-7mm [SZH-SUP01]	10	₩ 2,100
45	고무발 라디오발 옵션 선택 (S-1 / 18*10H)	10	₩ 600
46	5T 아크릴 검정 260*140 도면가공	1	₩ 8,000
47	3T 아크릴 검정 266*205 도면가공	1	₩ 8,000
48	3T 아크릴 검정 140*205 도면가공	2	₩ 3,200
49	2T 아크릴 검정 140*205 도면가공	1	₩ 1,900
50	너트 (니켈) M2	10	₩ 100
51	PCB 서포트 황동 2 파이 M-5mm	8	₩ 1,600
52	Total Tax Fee	9	₩ 9,504
53	Total Shipping Fee	14	₩ 50,308
54	Total Amount		₩ 256,424

Reference

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Q & A