광운튜터링
RTL CODING 실습
및
FPGA에 실제 IP 설계 (UART 송수신)

2023-12-26

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설계하는감자

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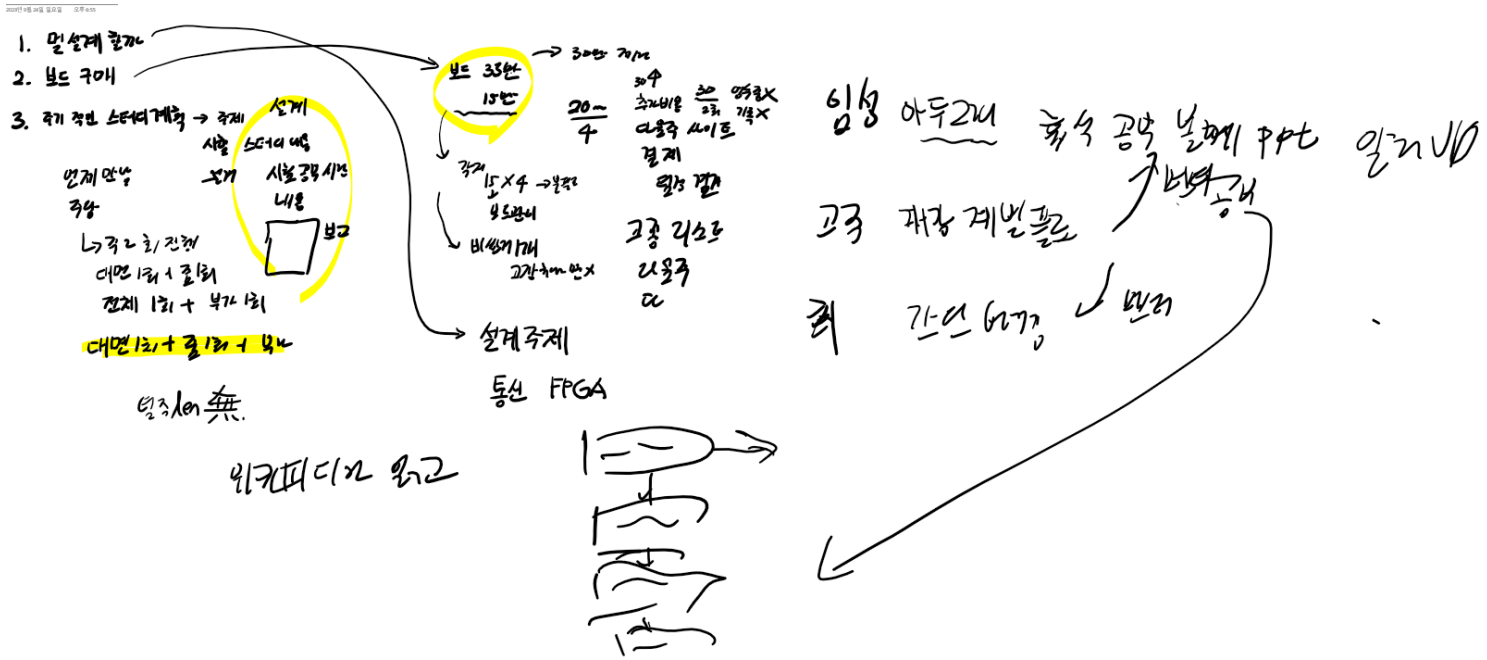
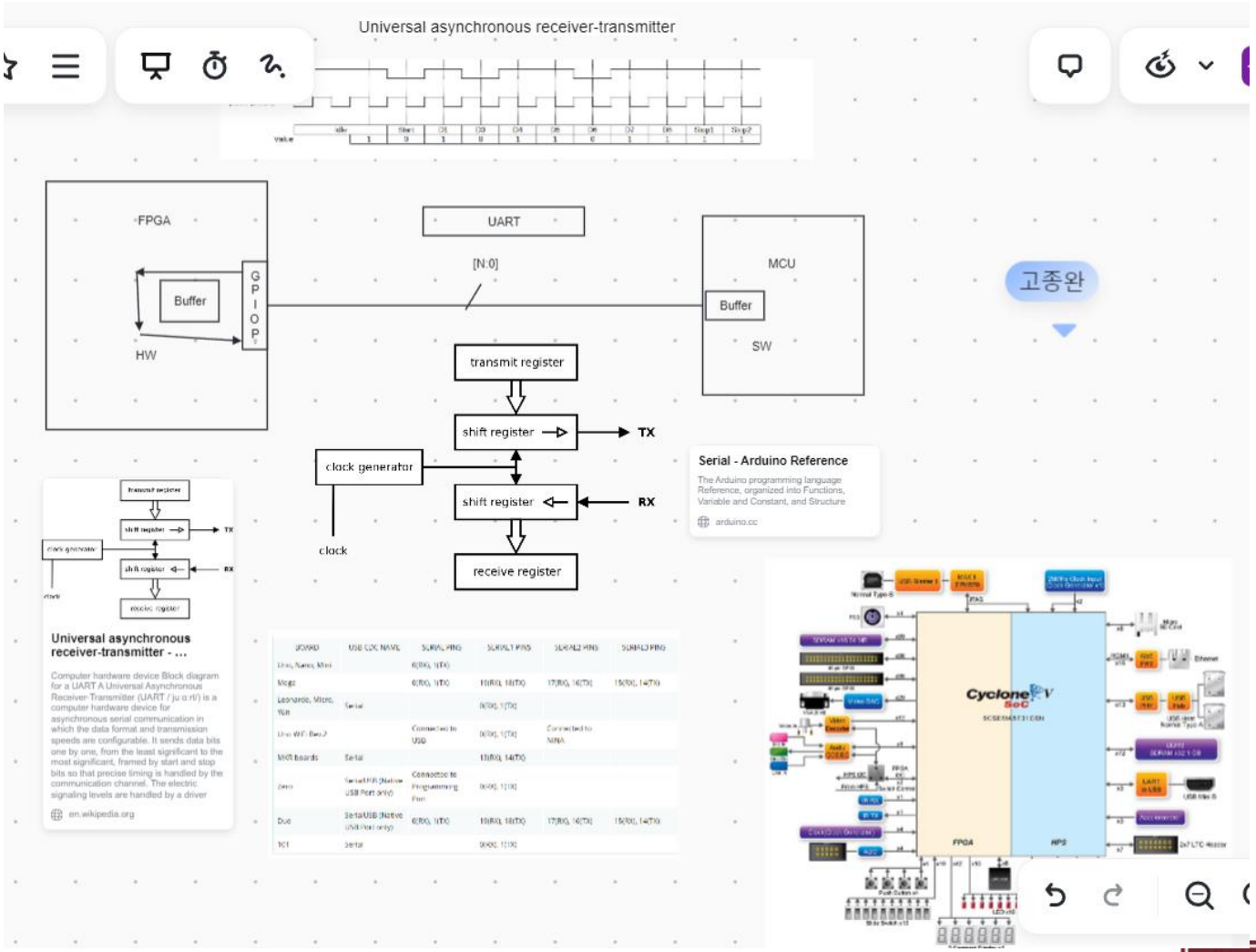
Brainstorming [Sept 18 – 24]

- Brainstorming to gather ideas for out project.



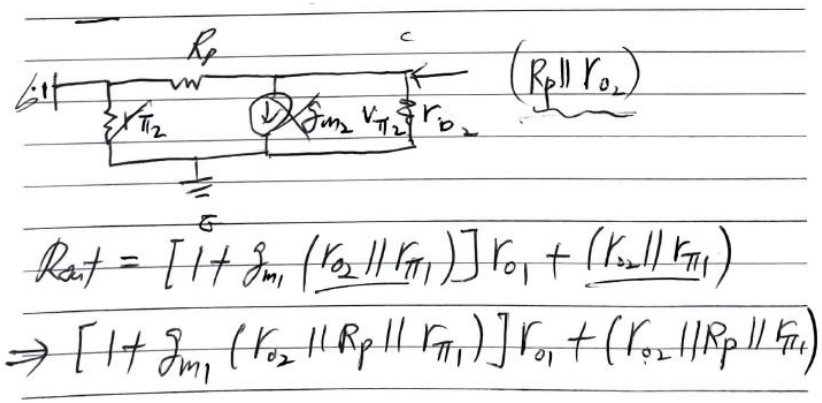
Specification of IP – UART [Sept 15 – Oct 1]

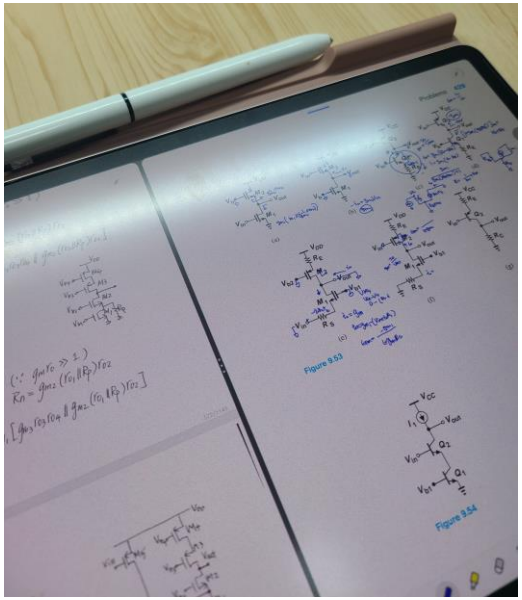
- Specifying IP for designing - UART



Specification of IP – UART [Oct 2– Oct 30]

- Studying basic concepts for Digital circuit designs.

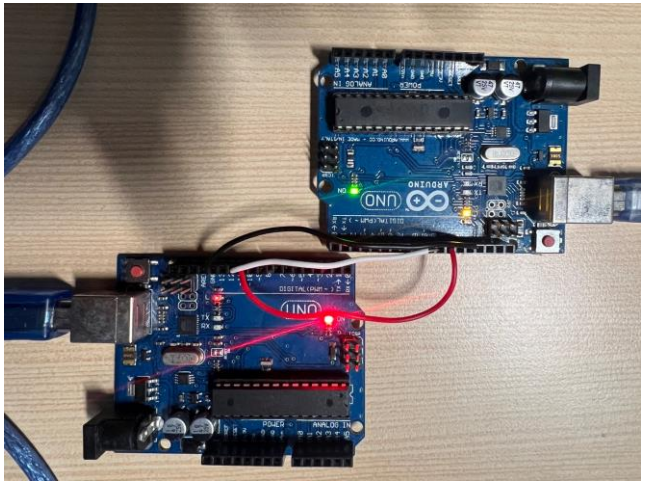


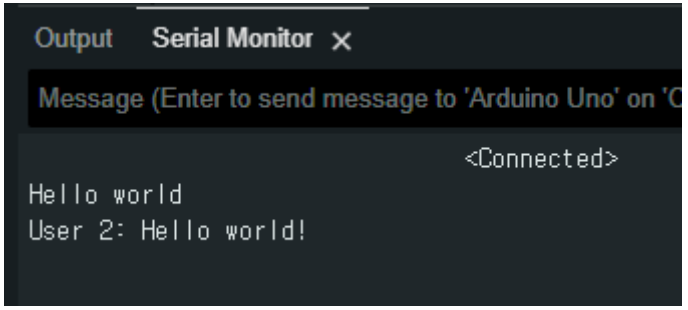


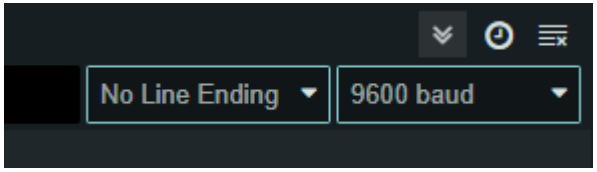
```
for (int i = 0 ; i < N ;i++)
{
for (int j = 0; j < N ; j++)
{
prove_row = i * scale_row;
prove_row_fall = std::floor(prove_row);
bilinear_row = prove_row - prove_row_fall;
prove_col = j * scale_col;
prove_col_fall = std::floor(prove_col);
bilinear_col = prove_col - prove_col_fall;
a = imageArray[prove_row_fall][prove_col_fall];
b = imageArray[prove_row_fall + 1][prove_col_fall];
c = imageArray[prove_row_fall][prove_col_fall +1];
d = imageArray[prove_row_fall + 1][prove_col_fall +1];
e = (b - a) * bilinear_row + a;
predictor_store[i][j] = ( ( (c - d - b - a)* bilinear_row + c - a ) * bilinear_col + e;
}}
```

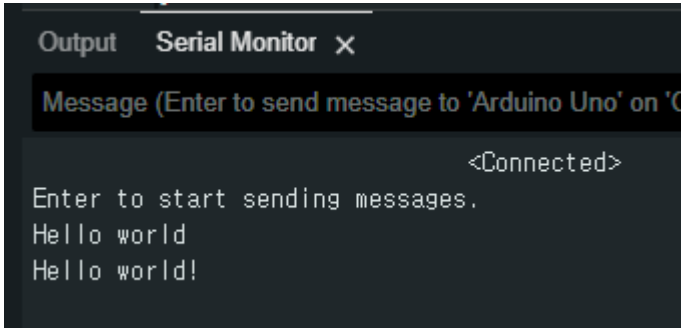
Simple Chatting program [Oct 31– Nov 02]

- Connect TX – RX and Ground pin.



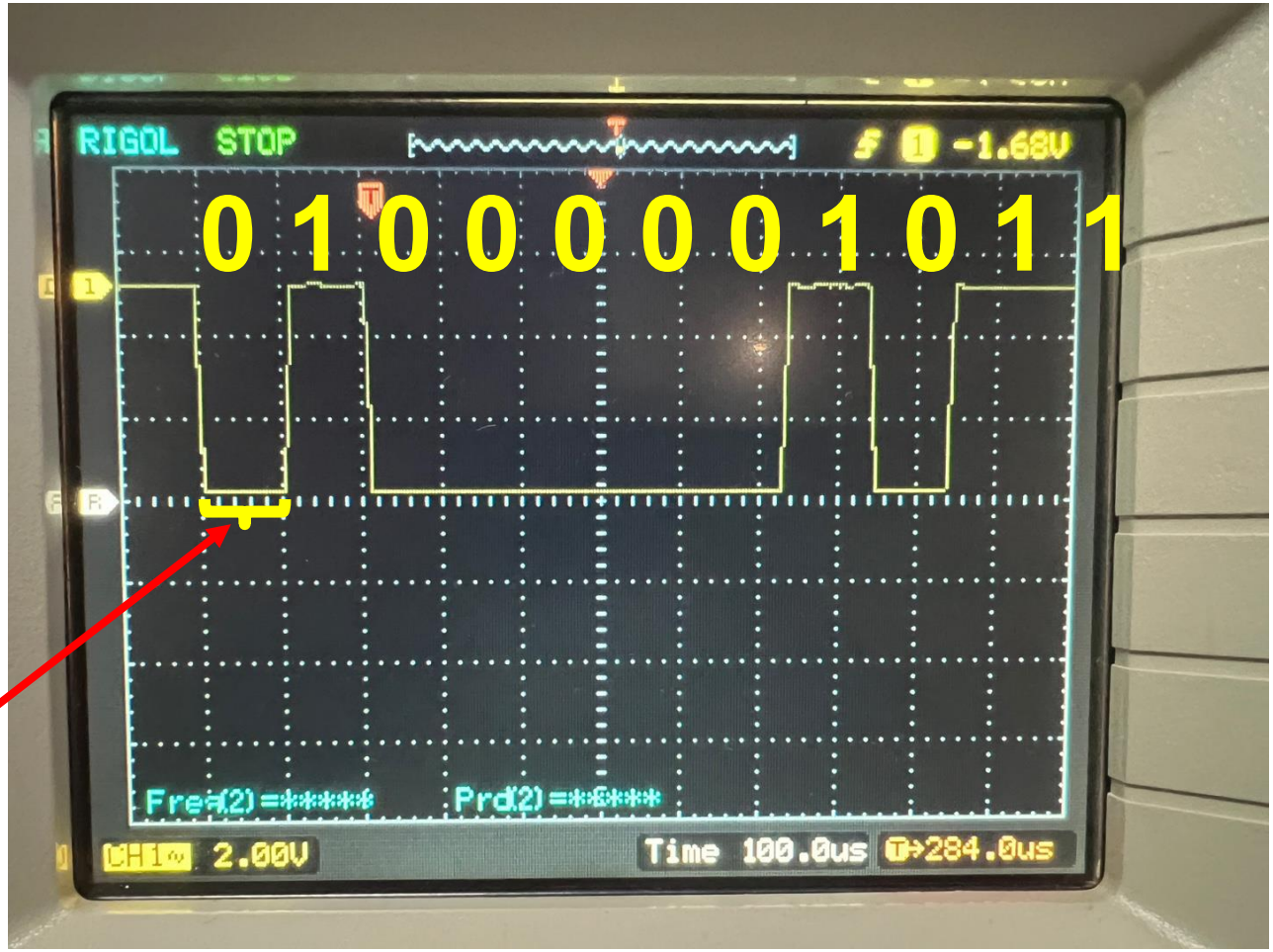






Capturing the Signal [Oct 31– Nov 02]

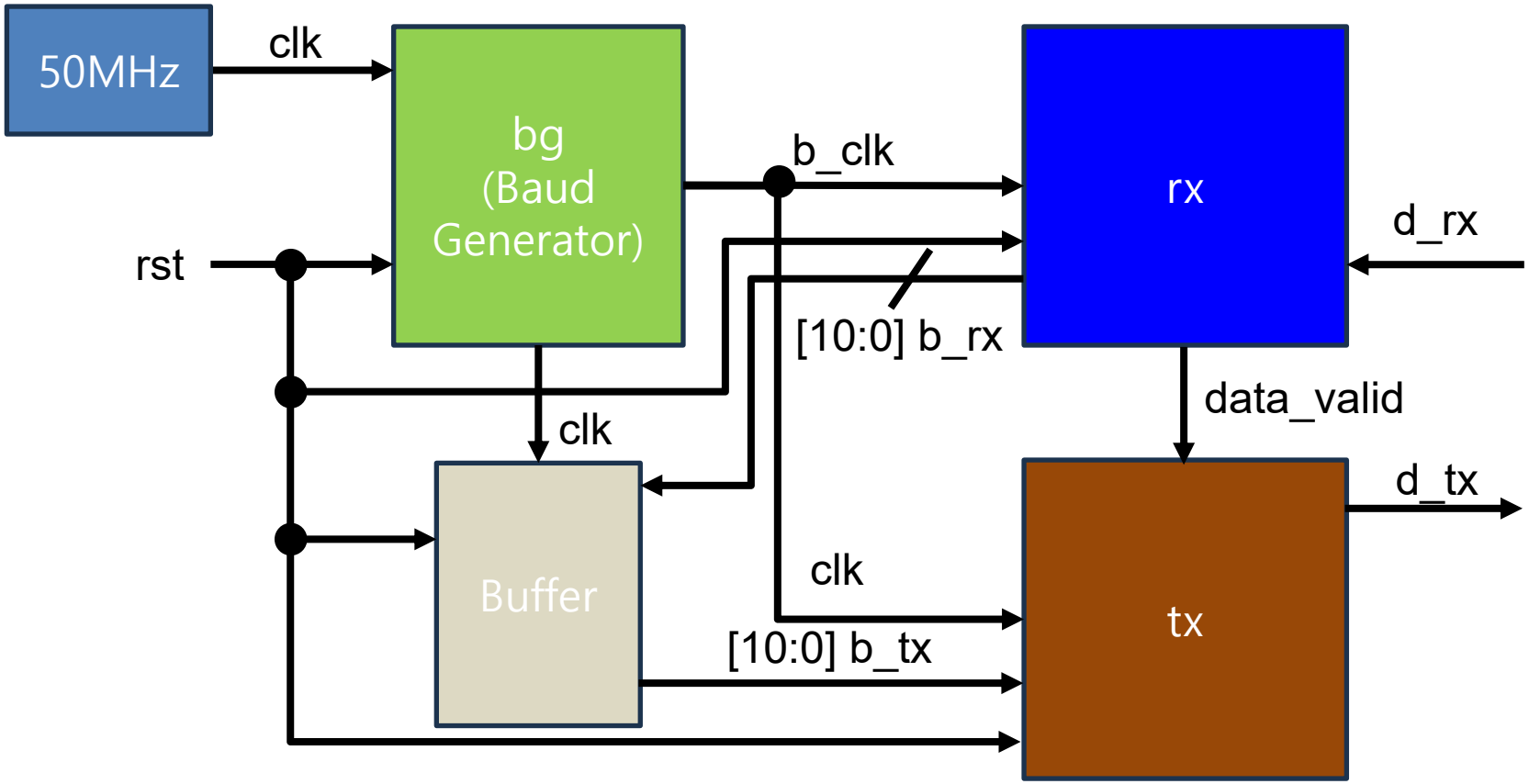
- Connect Tx and Ground to Probe.



1 Bit

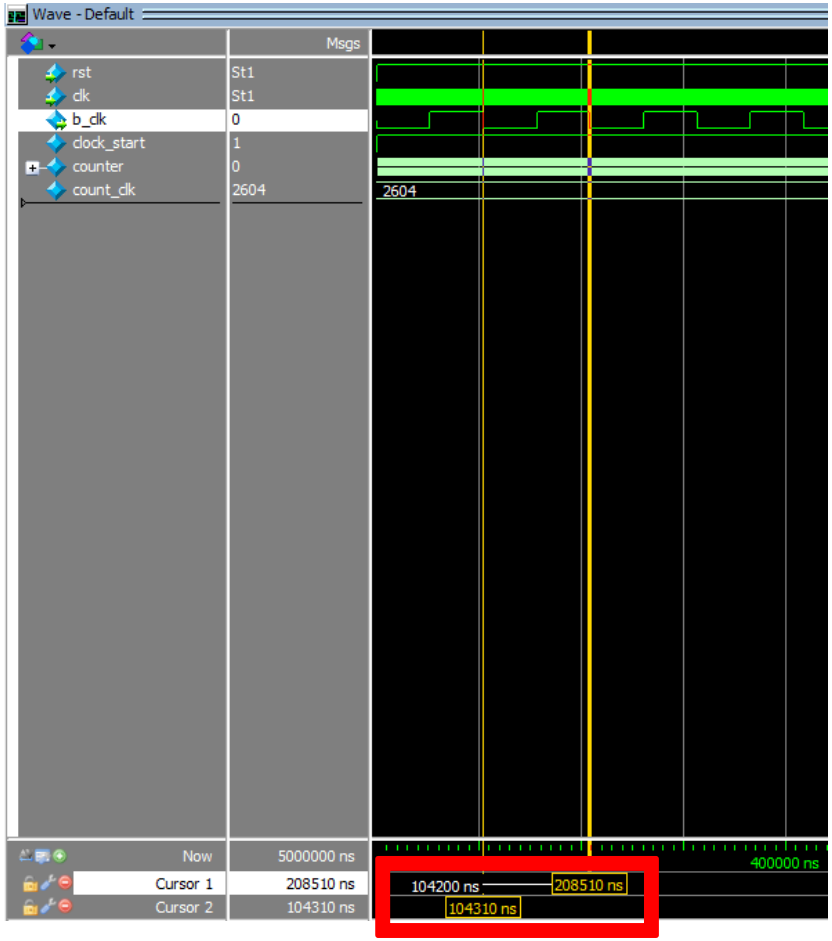
Hardware Implementation [Oct 3 – Oct 12]

- UART Block Diagram



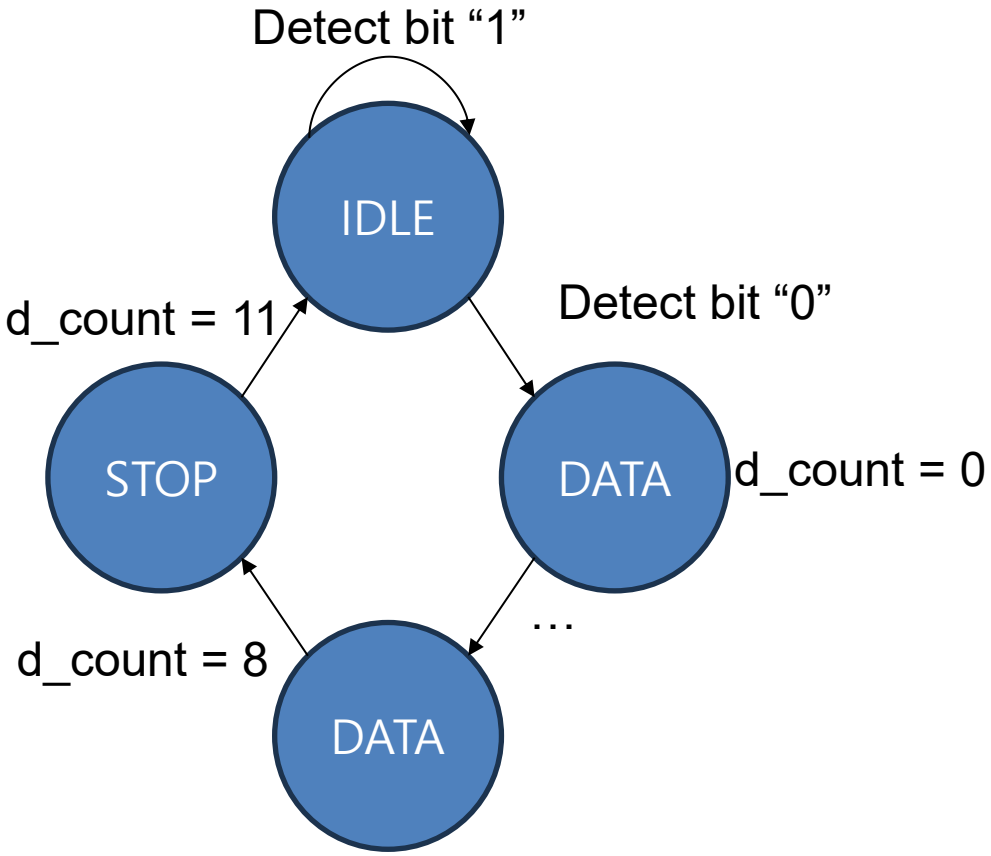
Hardware Implementation (Cont.) [Oct 3 – Oct 12]

- UART Baud Generator
  - 50Mhz input from FPGA Clock system => 0.02us.
  - 104.116us / 0.02us = 5208 counts to reset clock. (104.200us)



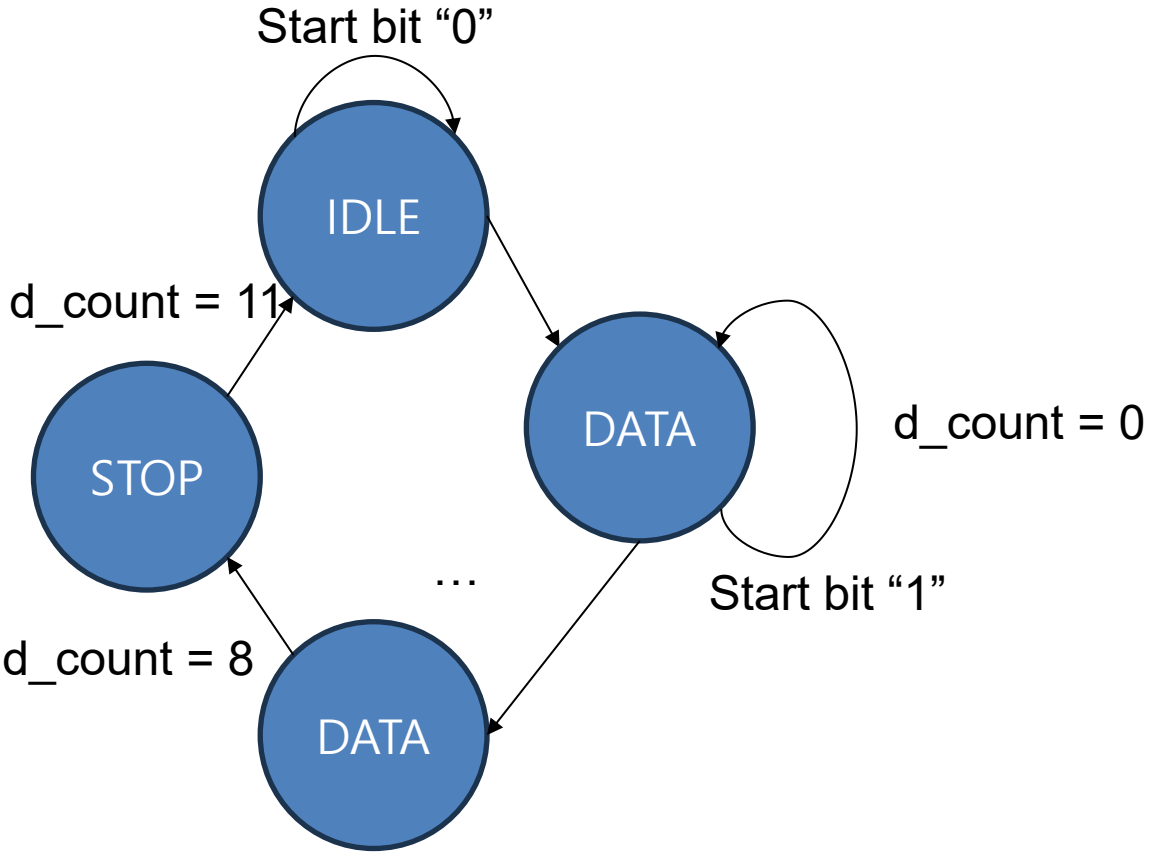
Hardware Implementation (Cont.) [Oct 3 – Oct 12]

- UART Receiver State Machine



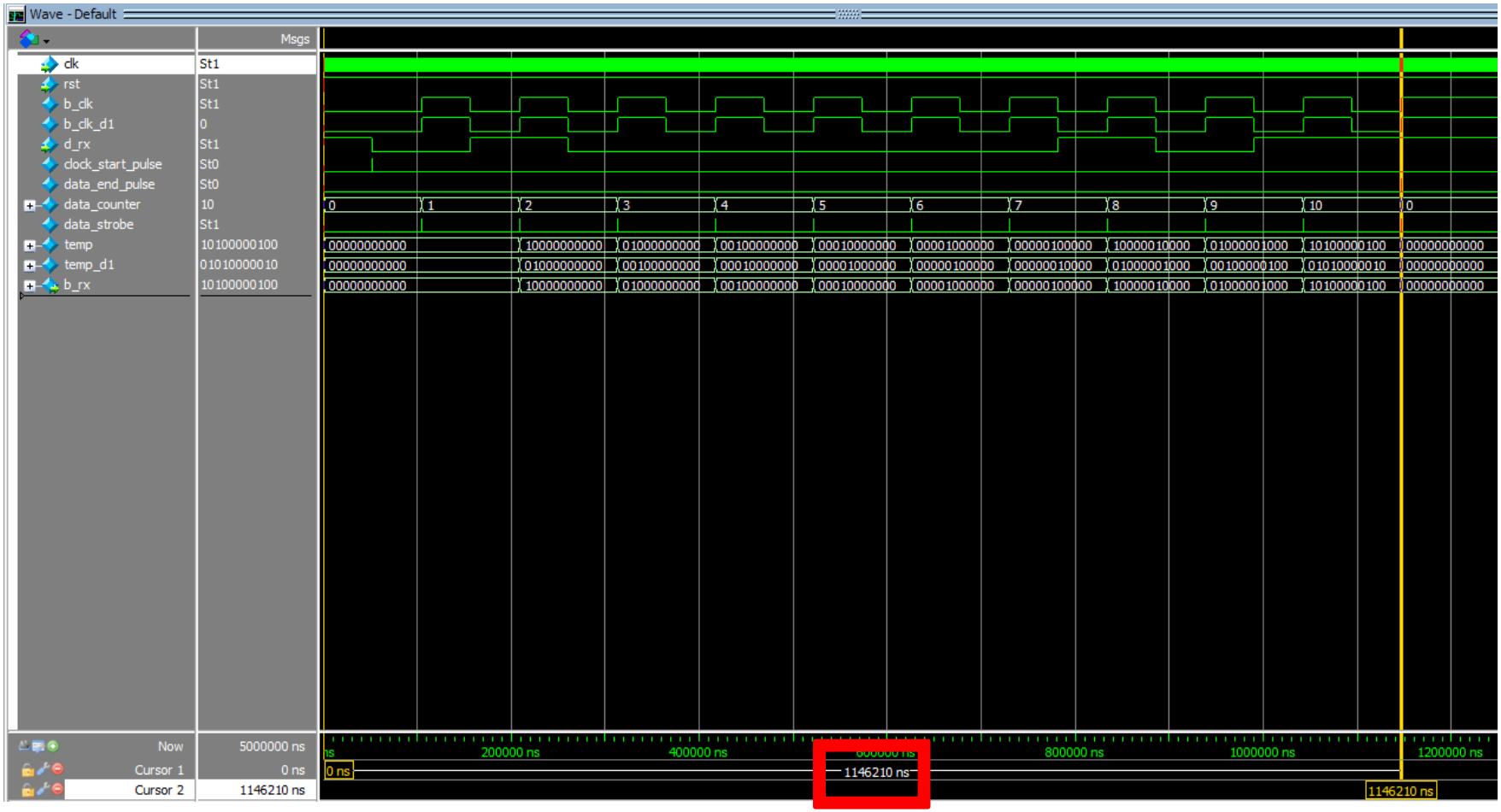
Hardware Implementation (Cont.) [Oct 3 – Oct 12]

- UART Transmitter State Machine



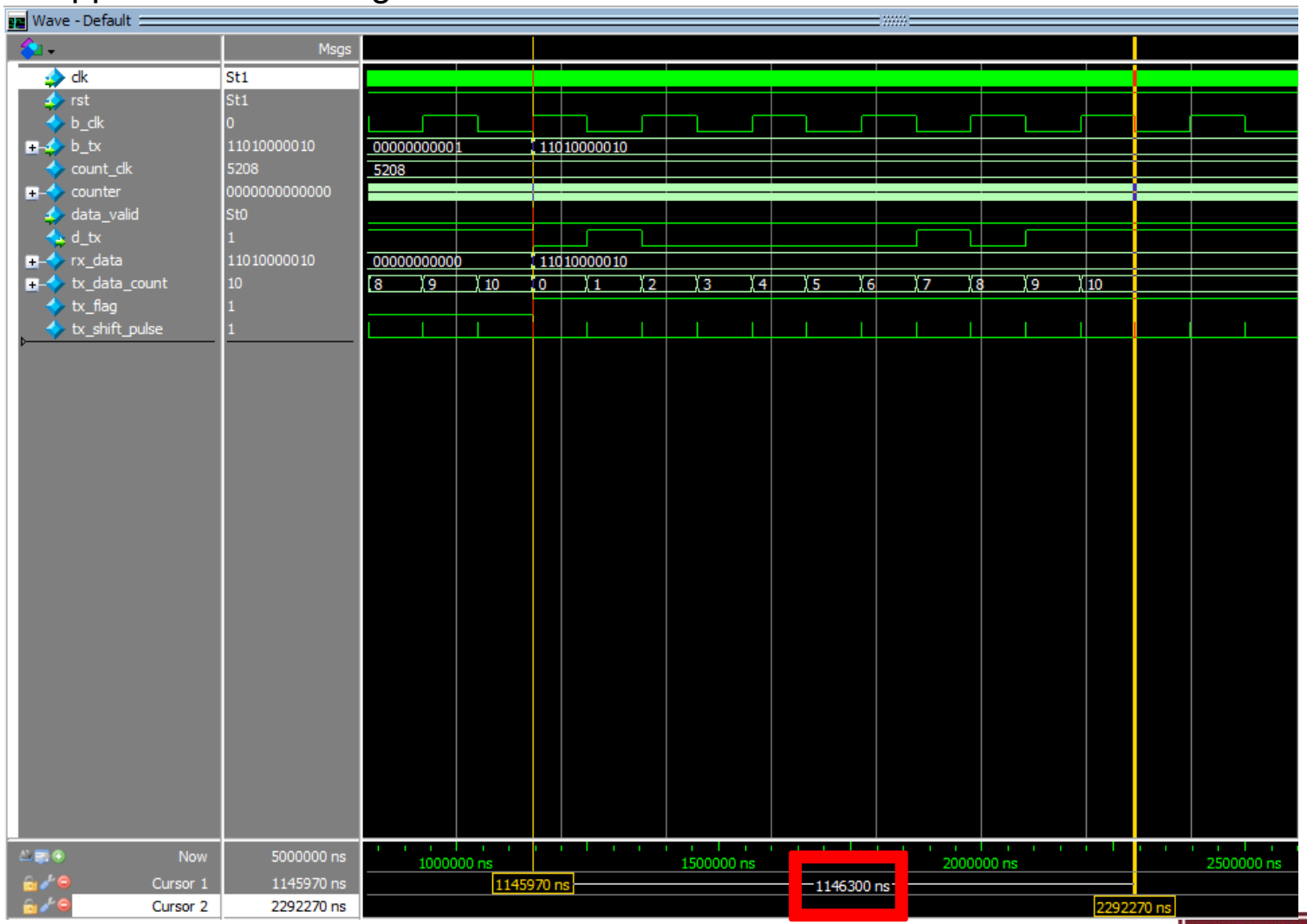
Receiver [Oct 3 – Oct 19]

- Uppercase A is being received.



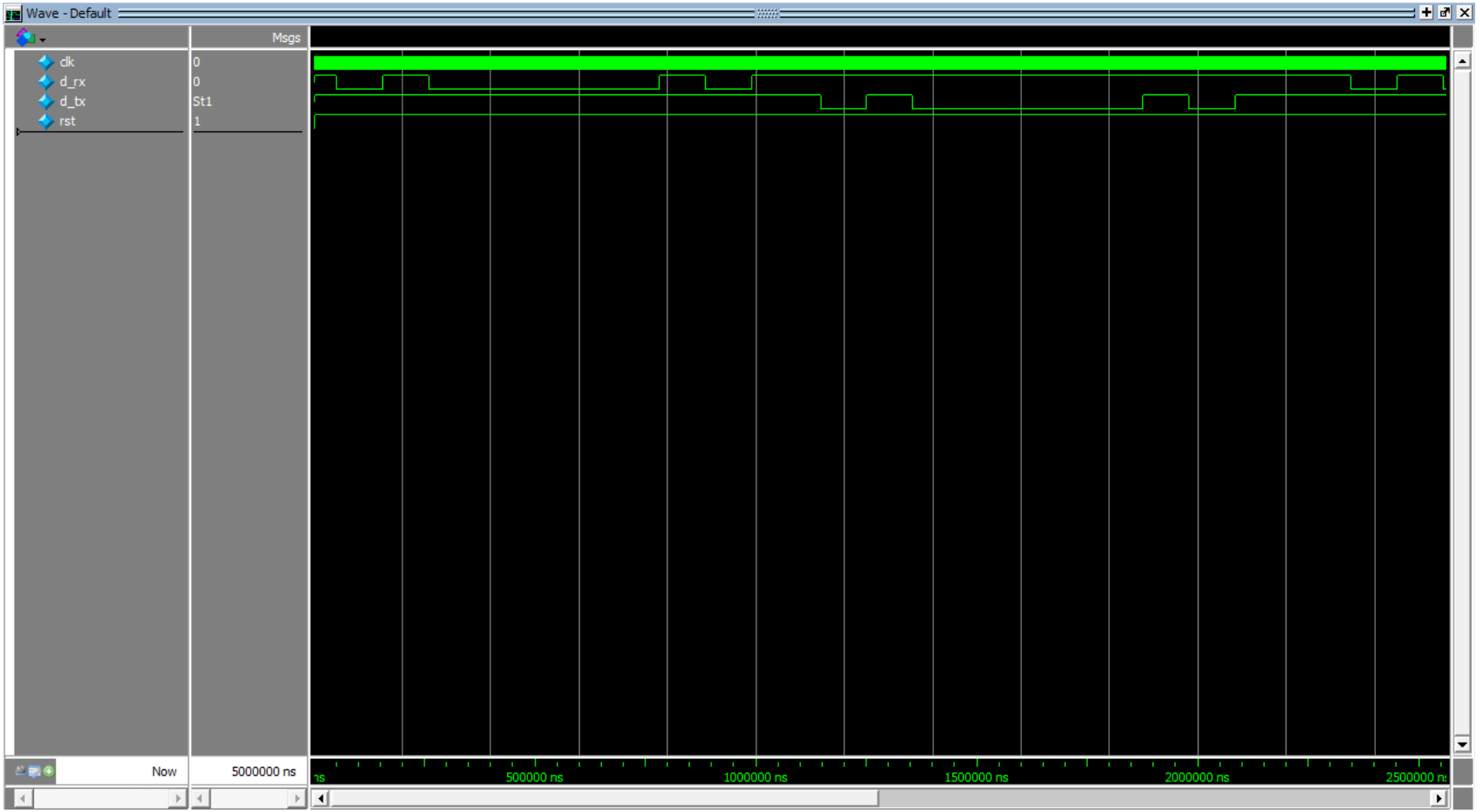
Transmitter [Oct 3 – Oct 19]

- Uppercase A is being transmitted



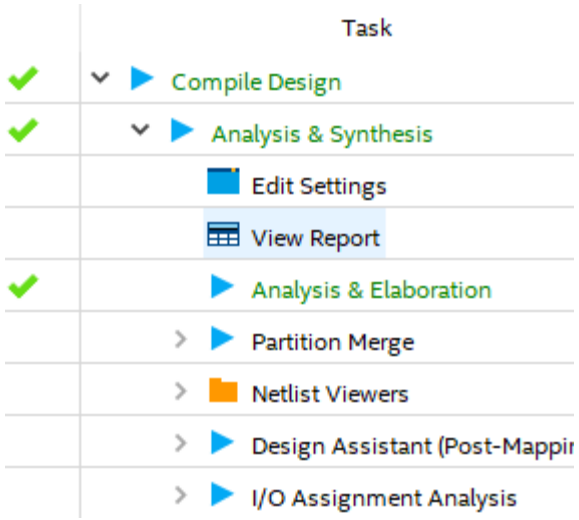
Top File [Oct 3 – Oct 19]

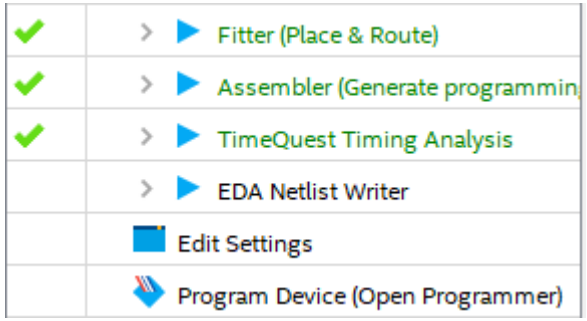
- Uppercase A is being received and transmitted

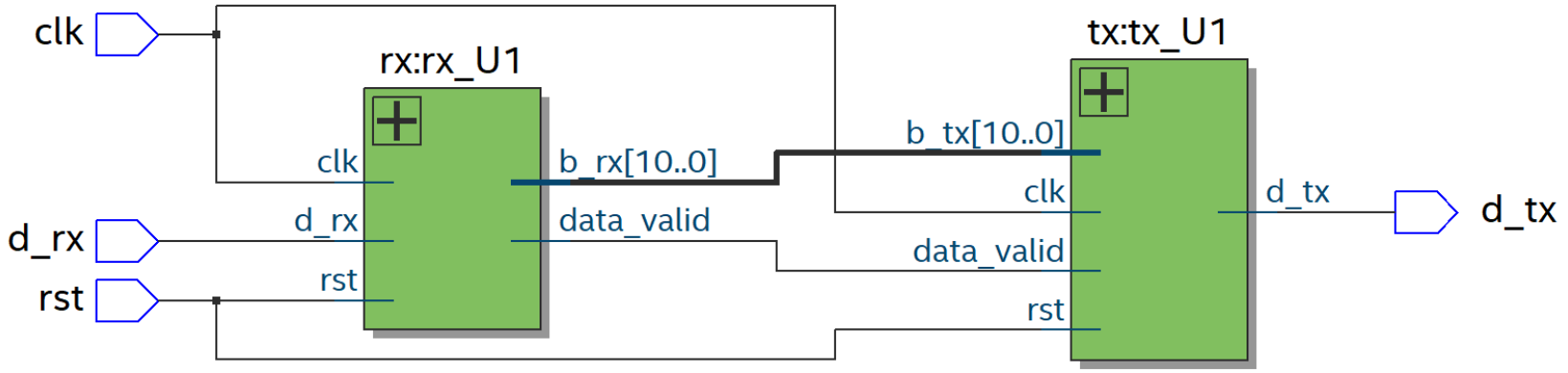


FPGA [Oct 20 – Oct 26]
(Quartus Synthesis and DE1-SoC board Upload)

- Synthesis

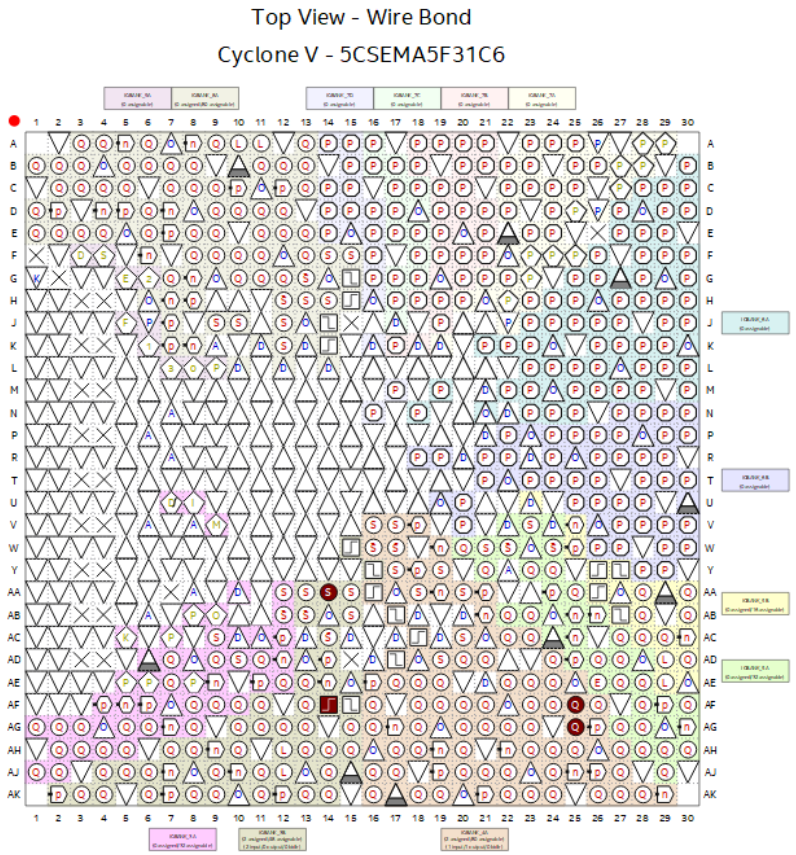






FPGA [Oct 20 – Oct 26]
(Quartus Synthesis and DE1-SoC board Upload)

- Pin planning.



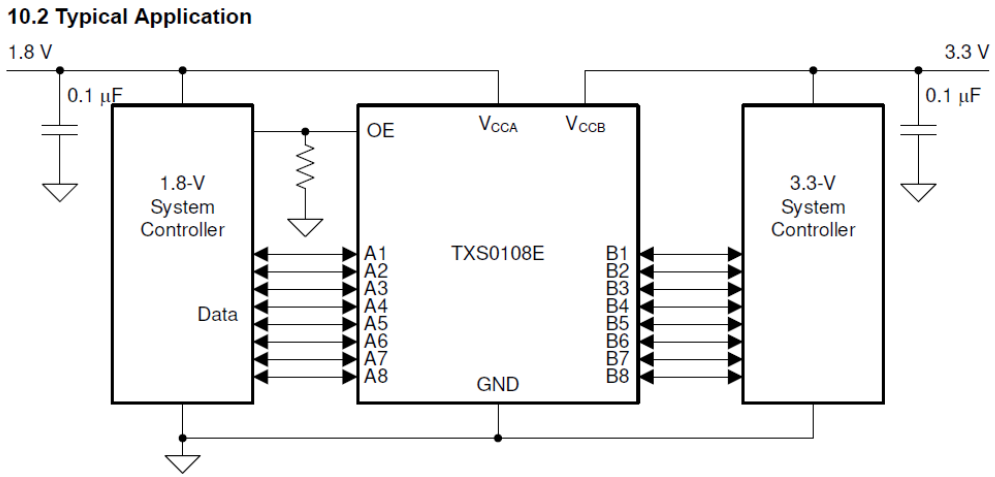
Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate
in clk	Input	PIN_AF14	3B	B3B_N0	PIN_Y27	2.5 V (default)		12mA (default)	
in d_rx	Input	PIN_AF25	4A	B4A_N0	PIN_AB28	2.5 V (default)		12mA (default)	
out d_tx	Output	PIN_AG25	4A	B4A_N0	PIN_AA28	2.5 V (default)		12mA (default)	1 (default)
in rst	Input	PIN_AA14	3B	B3B_N0	PIN_AC29	2.5 V (default)		12mA (default)	
<<new node>>									

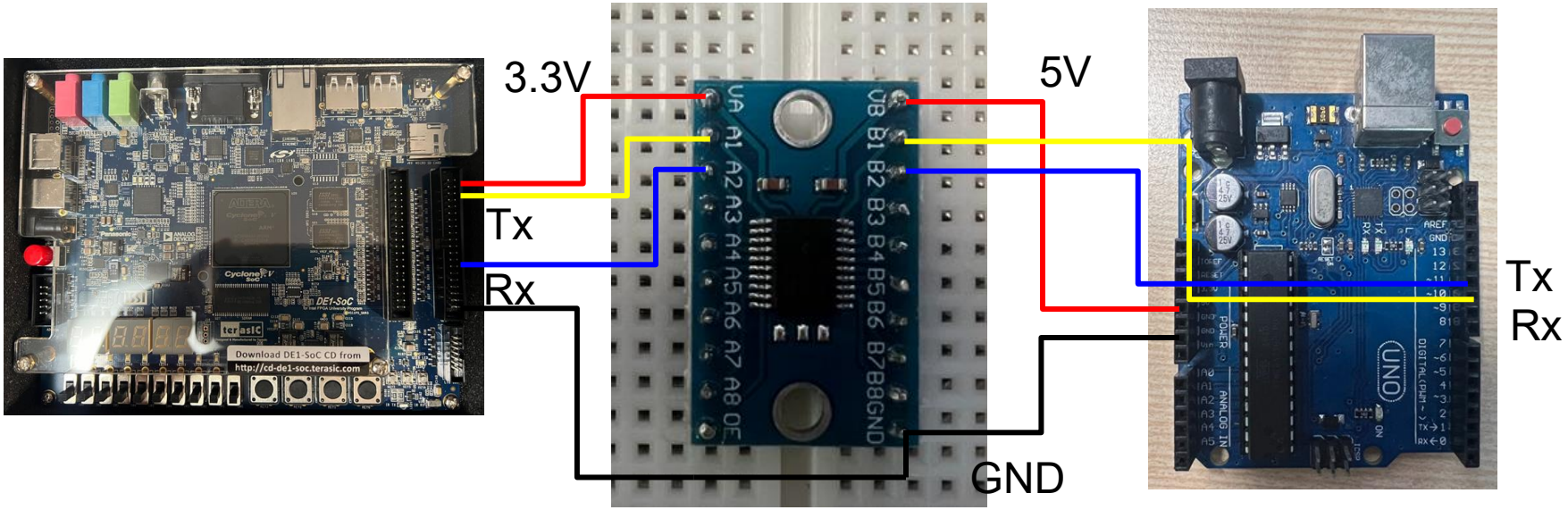
FPGA [Oct 20 – Oct 26]
(Quartus Synthesis and DE1-SoC board Upload)

- Summary

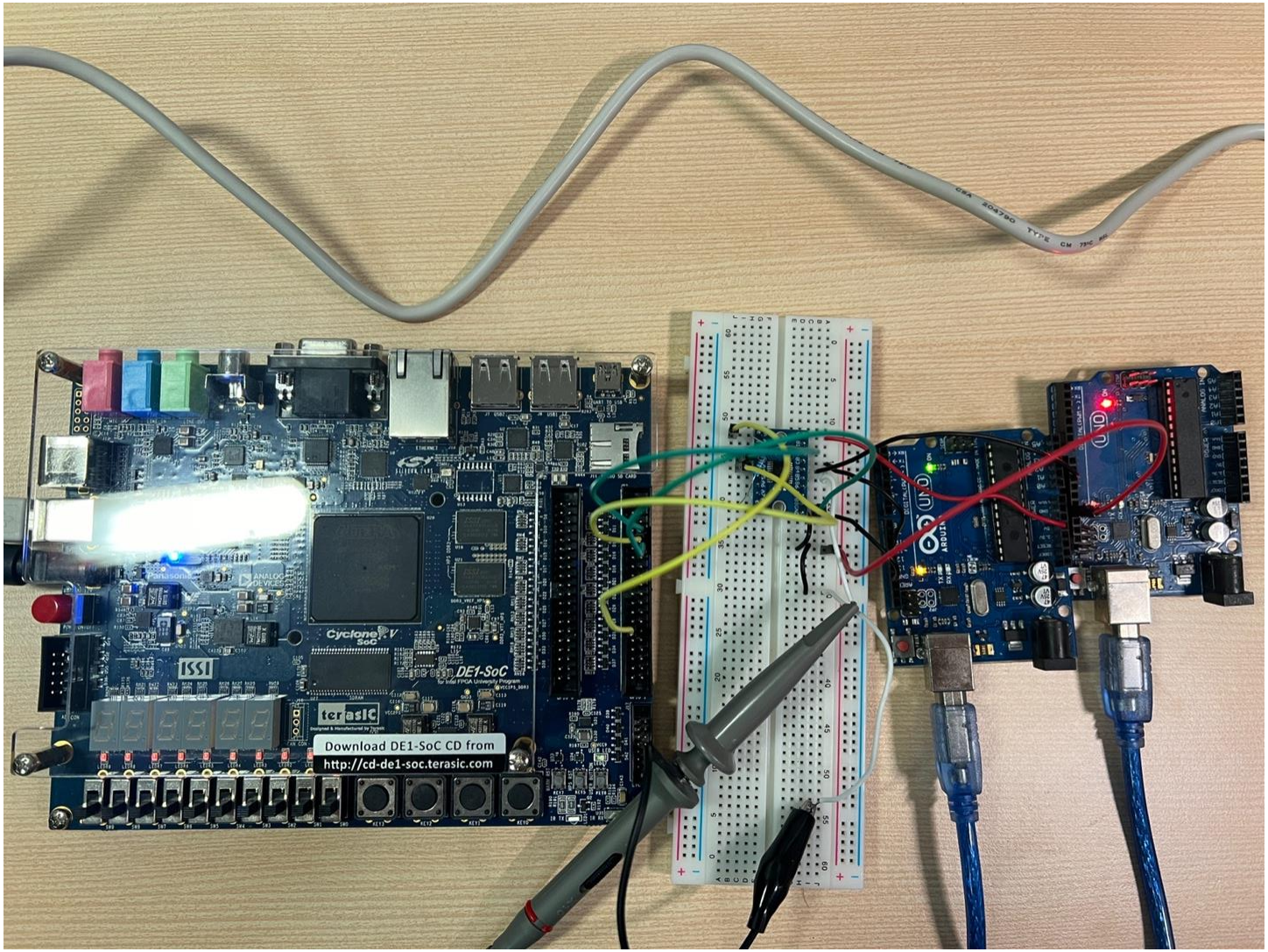
Flow Status	Successful - Sun Nov 12 20:34:08 2023
Quartus Prime Version	16.1.0 Build 196 10/24/2016 SJ Standard Edition
Revision Name	top_uart
Top-level Entity Name	top_uart
Family	Cyclone V
Device	5CSEMA5F31C6
Timing Models	Final
Logic utilization (in ALMs)	45 / 32,070 (< 1 %)
Total registers	102
Total pins	4 / 457 (< 1 %)
Total virtual pins	0
Total block memory bits	0 / 4,065,280 (0 %)
Total DSP Blocks	0 / 87 (0 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)

Chapter 5: Level Shifter (Cont.) [Oct 27 – Dec 17]

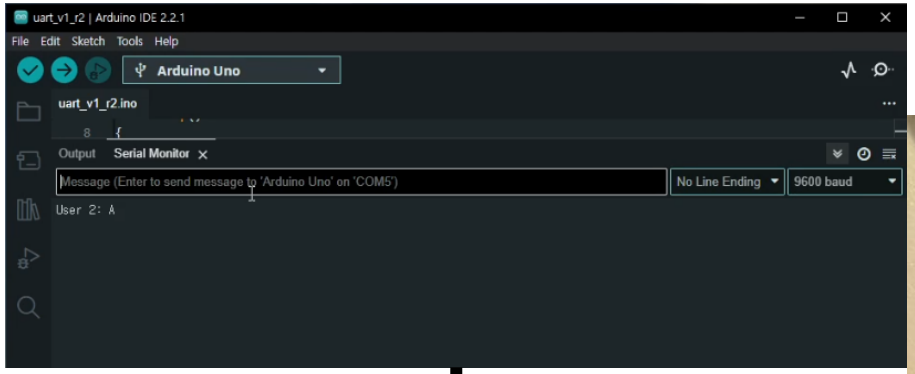




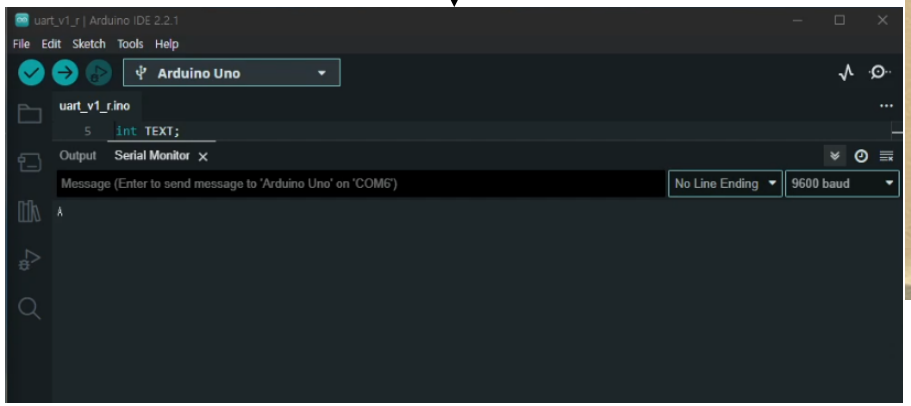
Project Integration [Oct 27 – Dec 17]

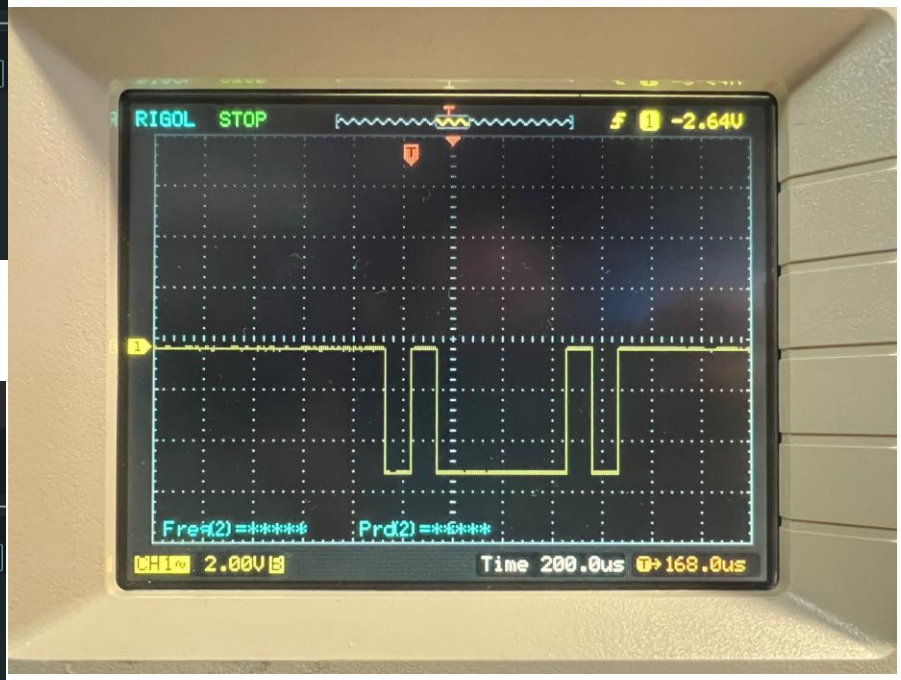


Project Integration [Oct 27 – Dec 17]



A





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Chapter 5: Result and Summary [Oct 27 – Dec 17]

```
vlog *.v
Model Technology ModelSim - Intel FPGA Edition vlog 10.5b Compiler 2016.10 Oct  5 2016
-- Compiling module bg
-- Compiling module rx
-- Compiling module tb_rx
-- Compiling module tb_top_uart
-- Compiling module top_uart
-- Compiling module tx

Top level modules:
        tb_rx
        tb_top_uart
End time: 23:46:16 on Nov 12,2023, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
```

Not Synthesizable

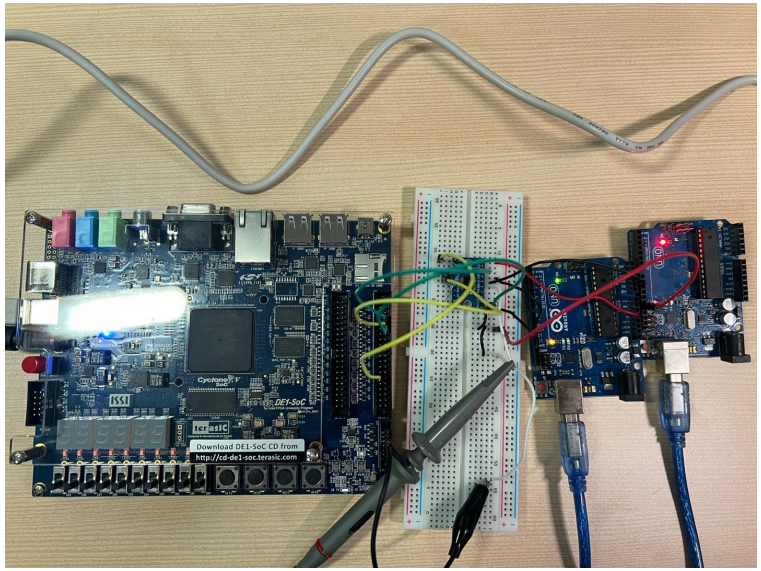
Type	ID	Message
ℹ		Running Quartus Prime Analysis & Synthesis
ℹ		Command: quartus_map --read_settings_files=on --write_settings_files=off to
⚠	18236	Number of processors has not been specified which may cause overloading on
ℹ	20030	Parallel compilation is enabled and will use 4 of the 4 processors detected
ℹ	12021	Found 1 design units, including 1 entities, in source file /verilog/uart/r_
ℹ	12021	Found 1 design units, including 1 entities, in source file /verilog/uart/r_
ℹ	12021	Found 1 design units, including 1 entities, in source file /verilog/uart/r_
ℹ	12021	Found 1 design units, including 1 entities, in source file /verilog/uart/r_
⚠	10236	Verilog HDL Implicit Net warning at top_uart.v(15): created implicit net fo
ℹ	12127	Elaborating entity "top_uart" for the top level hierarchy
ℹ	12128	Elaborating entity "rx" for hierarchy "rx:rx_U1"
⚠	10036	Verilog HDL or VHDL warning at rx.v(29): object "t" assigned a value but ne
ℹ	12128	Elaborating entity "bg" for hierarchy "rx:rx_U1|bg:u_bg"
ℹ	12128	Elaborating entity "tx" for hierarchy "tx:tx_U1"
✖	10028	Can't resolve multiple constant drivers for net "d_tx" at tx.v(136)
✖	10029	Constant driver at tx.v(122)
✖	12152	Can't elaborate user hierarchy "tx:tx_U1"
✖		Quartus Prime Analysis & Synthesis was unsuccessful. 3 errors, 3 warnings
✖	293001	Quartus Prime Full Compilation was unsuccessful. 5 errors, 3 warnings

```verilog
// data output
always @(posedge clk, negedge rst) begin
    if(!rst) begin
        d_tx <= 1'b1;
    end

    else if (tx_flag && (counter == 13'b1)) begin
        d_tx <= rx_data[tx_data_count];
    end

    else
        d_tx <= d_tx;
end

/*
always @(posedge clk, negedge rst) begin
    if(!rst) begin
        d_tx <= 1'b1;
    end

    else if (tx_flag) begin
        d_tx <= rx_data[0];
    end

    else
        d_tx <= 1'b1;
end
*/
```

Result and Summary [Oct 27 – Dec 17]

- Future improvements
  - Loop back on one Arduino.
  - Able to transmit more than one character.

- Overview of project
  - Could understand the fundamentals of communications.
  - Understand the basic theories in action.(Nyquist Theorem, RS232…)
  - Improve the use of an oscilloscope.(How to trigger Signals.)



Reference

- UART Diagram, https://en.wikipedia.org/wiki/Universal_asynchronous_receiver-transmitter#:~:text=A%20Universal%20Asynchronous%20Receiver%2DTransmitter,and%20transmission%20speeds%20are%20configurable.
- Example of 8 – QAM, https://www.wevolver.com/article/baud-rates-the-most-common-baud-rates
- ASCII code, https://web.alfredstate.edu/faculty/weimandn/miscellaneous/ascii/ascii_index.html
- Arduino Uno pinouts, https://docs.arduino.cc/hardware/uno-rev3
- Arduino Uno Schematics, https://www.arduino.cc/en/uploads/Main/Arduino_Uno_Rev3-schematic.pdf
- ATmega16U2 Datasheet, https://ww1.microchip.com/downloads/en/DeviceDoc/doc7799.pdf
- RS232 Connector, https://www.virtual-serial-port.org/article/what-is-serial-port/rs232-pinout/
- De1-SoC Schematic, https://people.ece.cornell.edu/land/courses/ece5760/DE1_SOC/DE1-SoC%20schematic.pdf
- De1-SoC Manual, https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=205&No=836&PartNo=4#contents
- Level Shifter, https://www.ti.com/lit/ds/symlink/txs0108e.pdf?ts=1699758033742

Q & A